

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

FIG.1

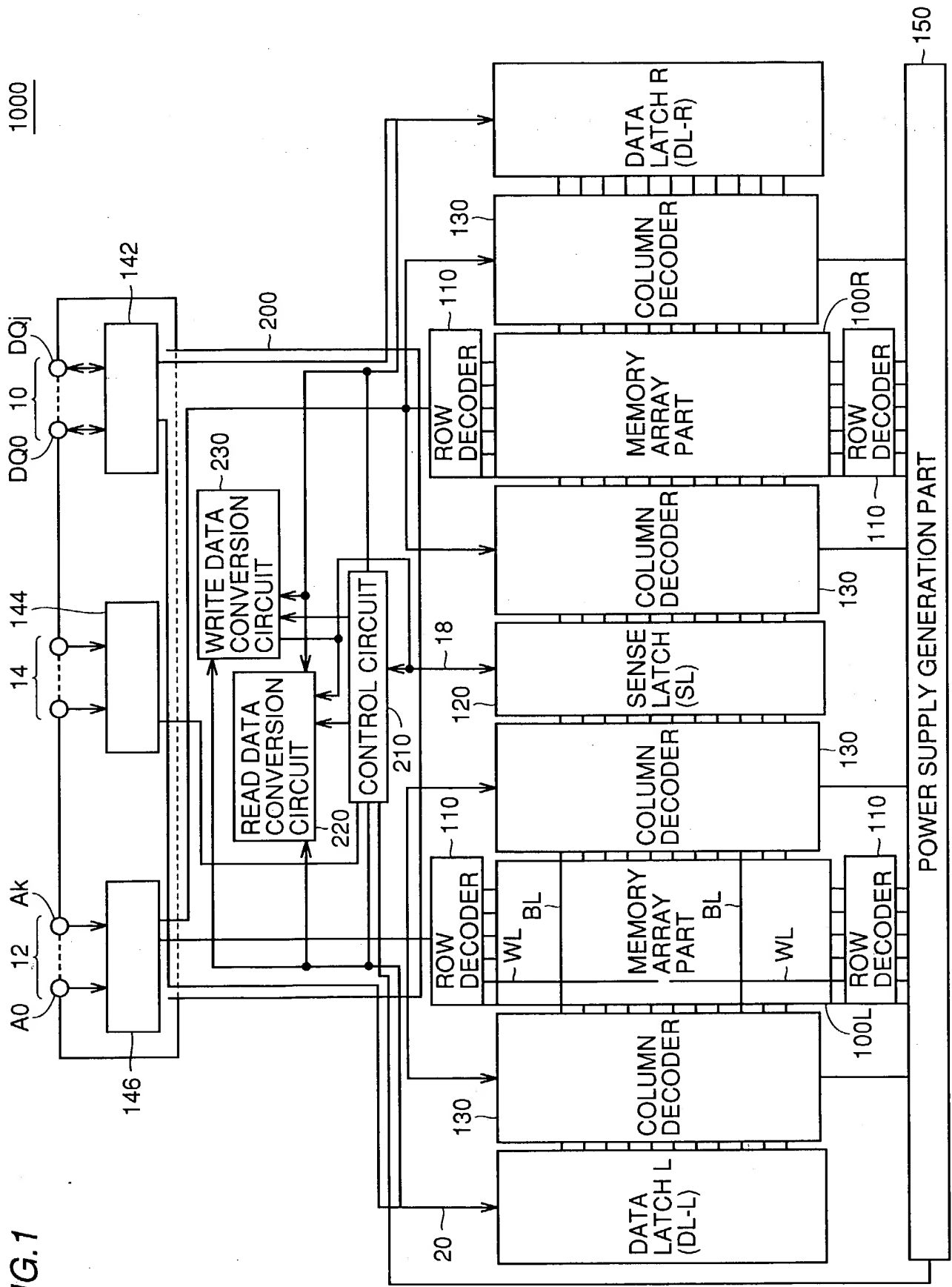


FIG.2

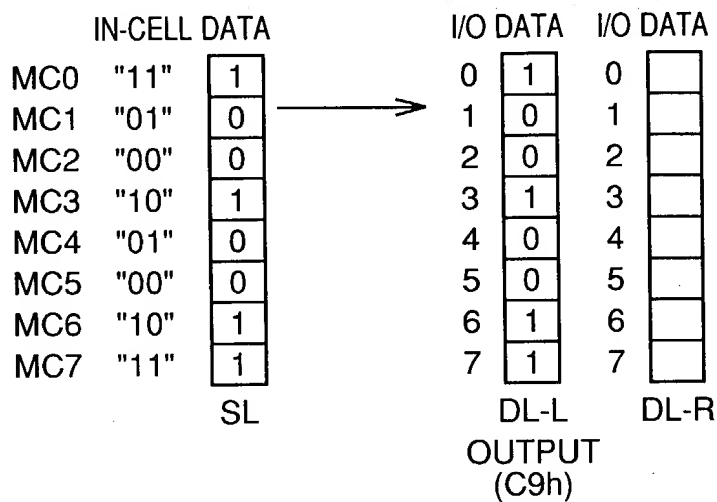


FIG.3

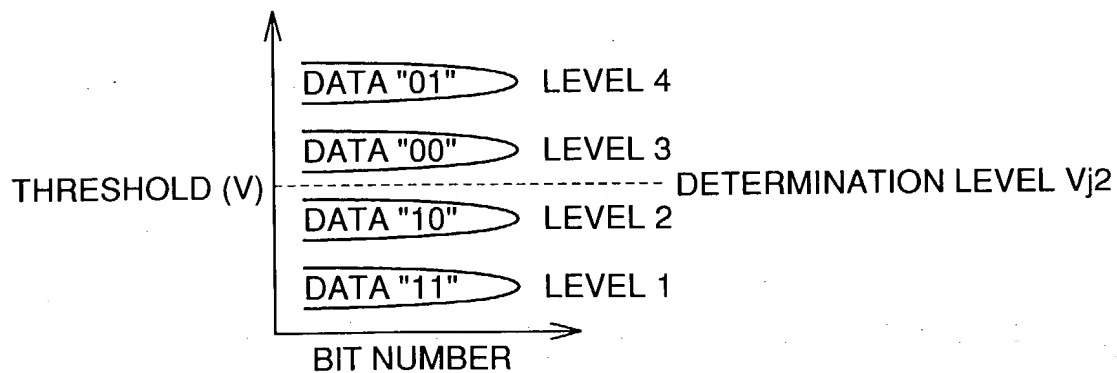


FIG.4

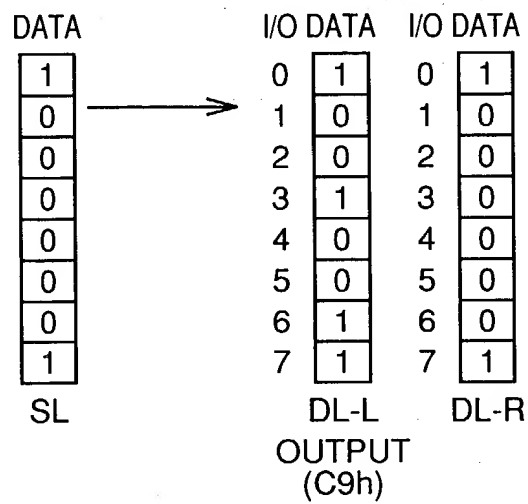


FIG.5

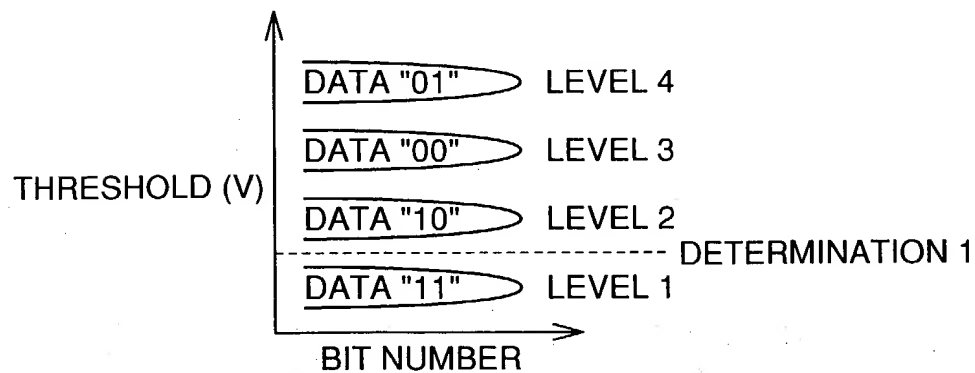


FIG. 6

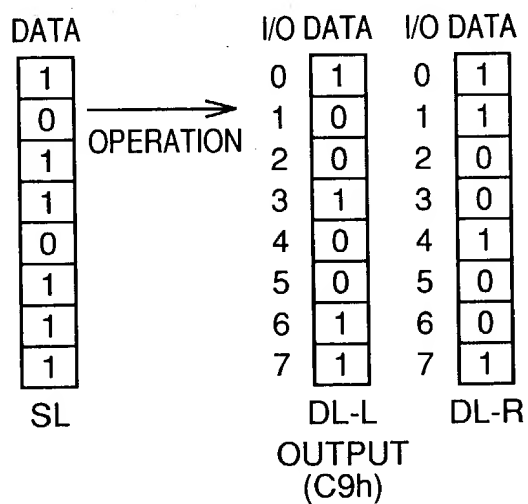


FIG. 7

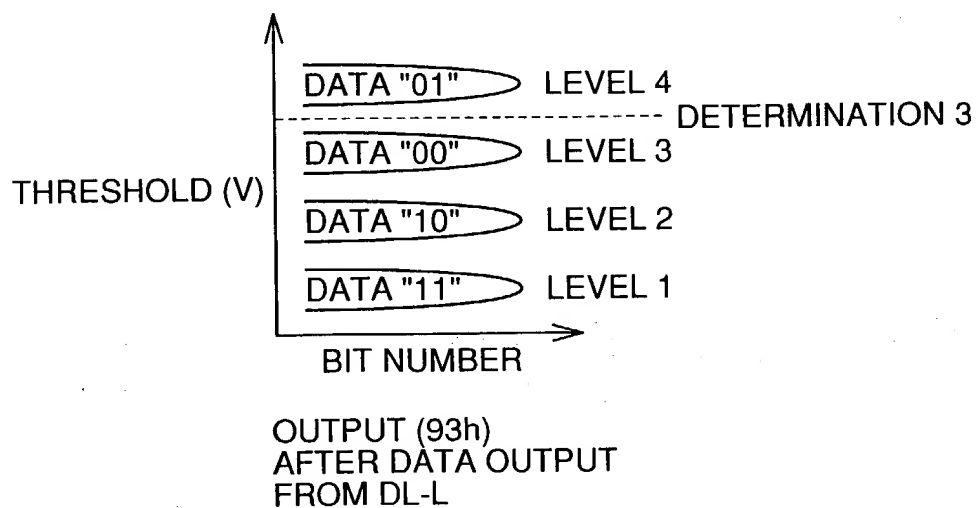


FIG. 8

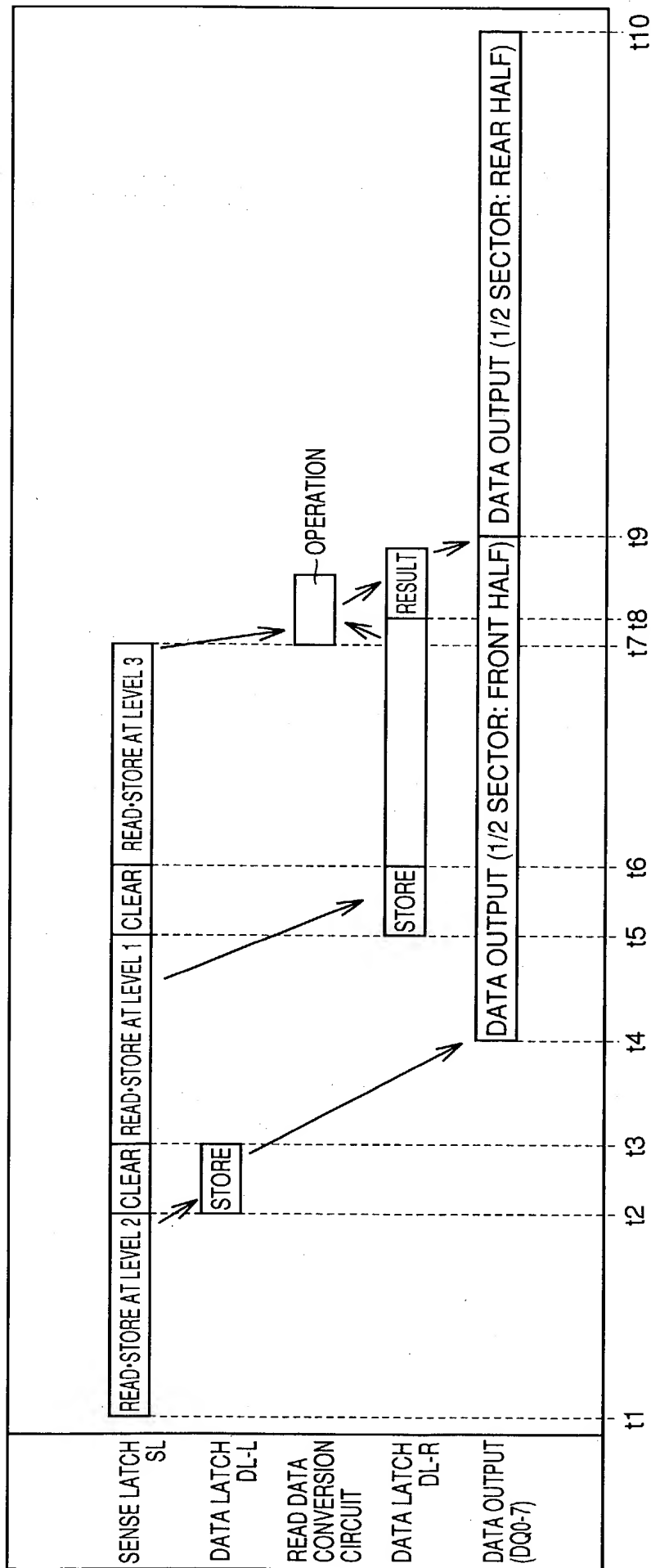


FIG.9

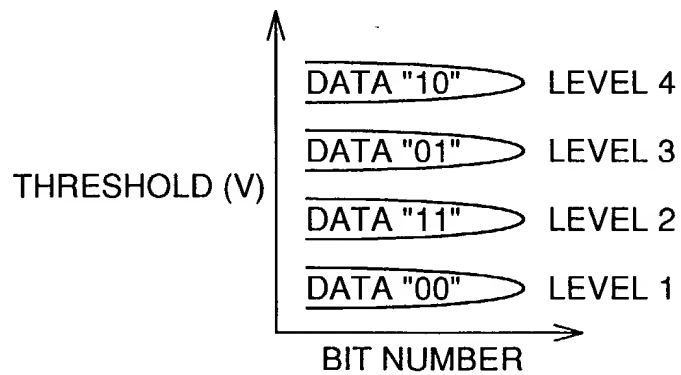


FIG.10

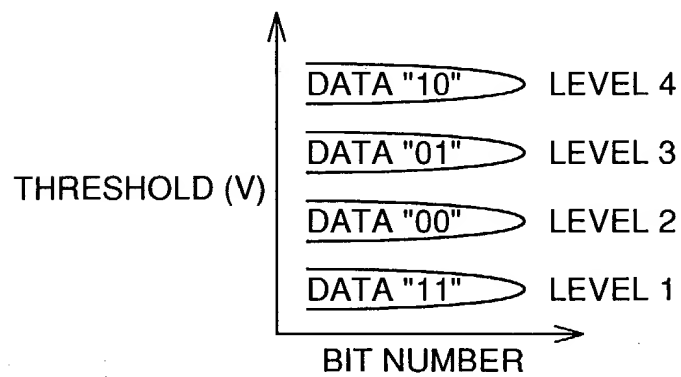


FIG.11

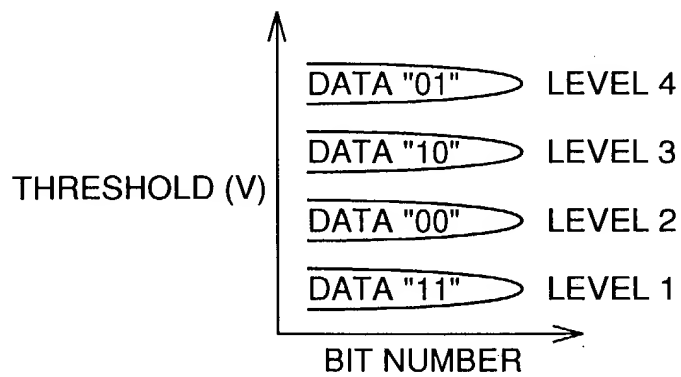


FIG.12

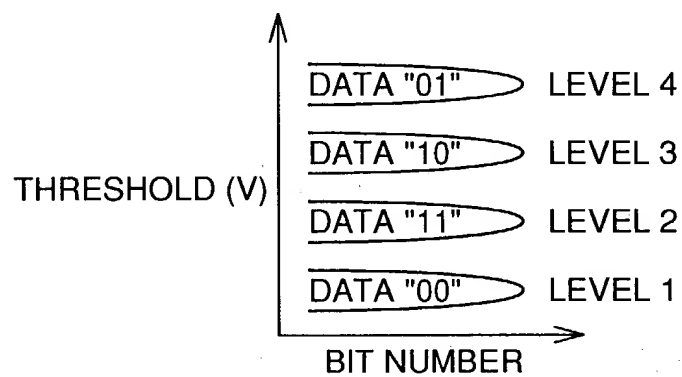


FIG.13

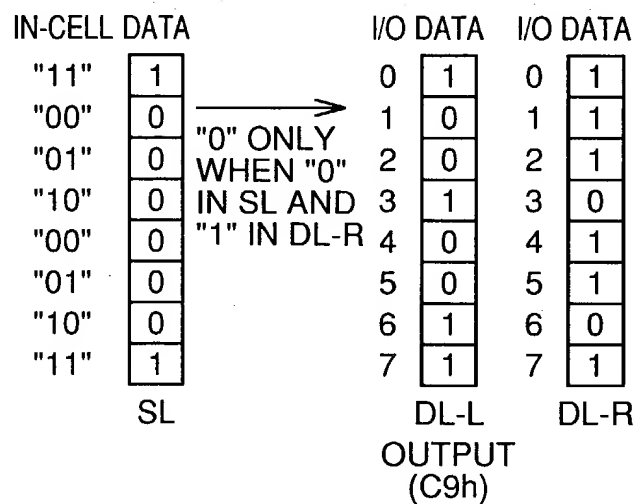


FIG.14

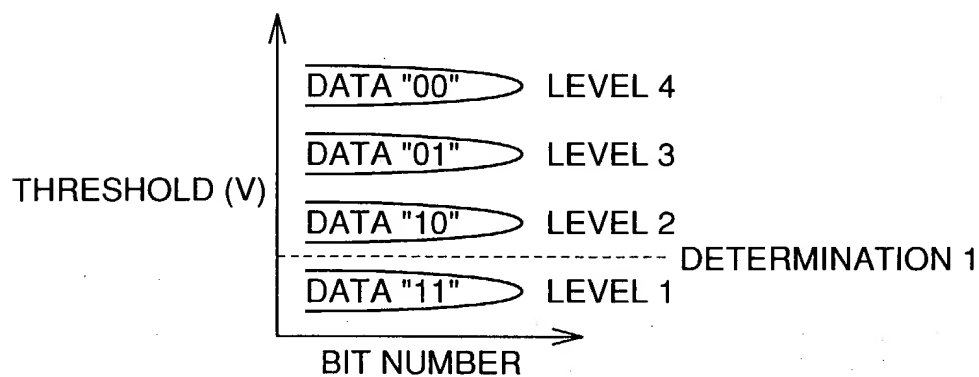


FIG.15

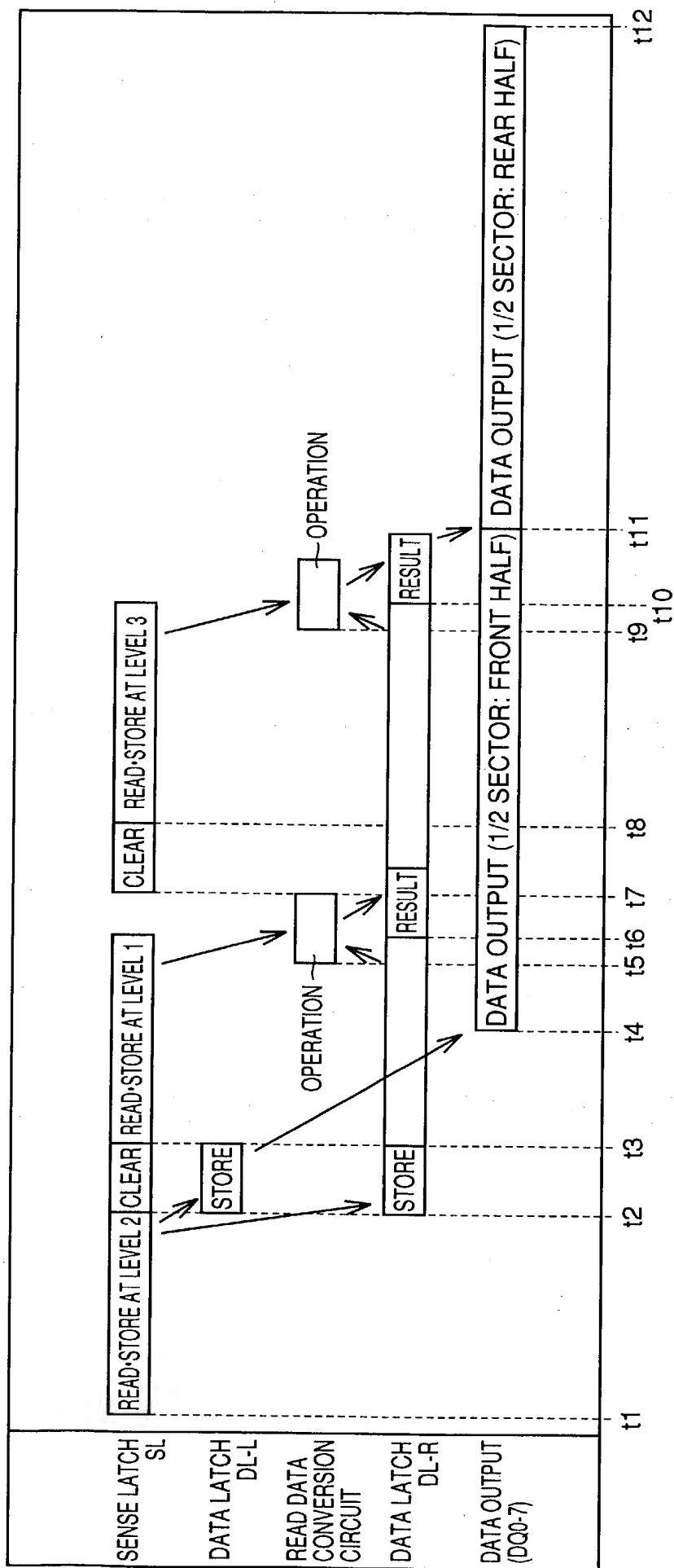


FIG. 16A

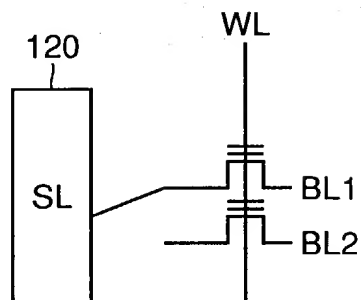


FIG. 16B

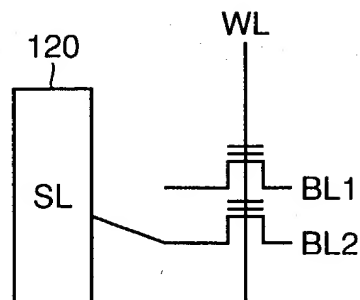


FIG. 17

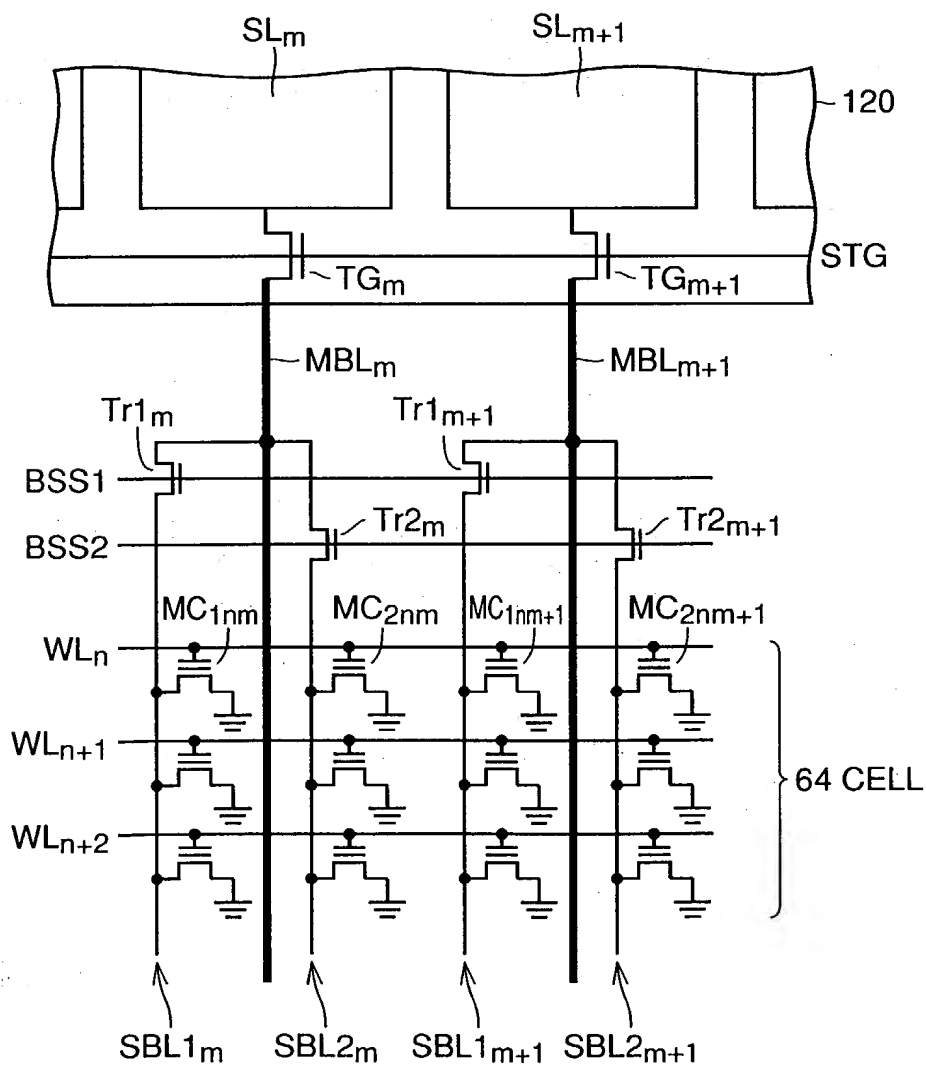


FIG. 18

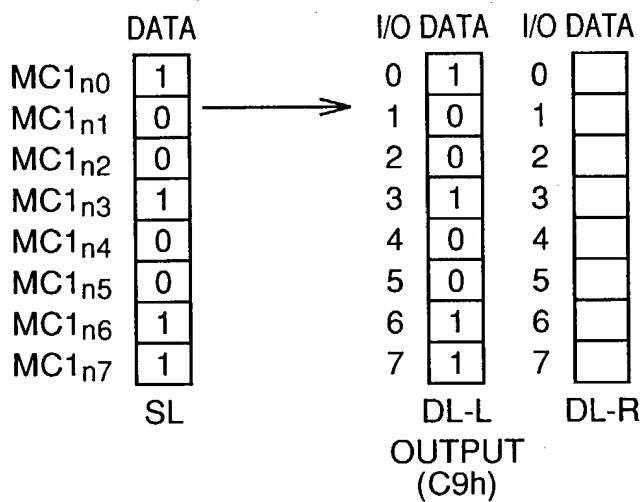


FIG. 19

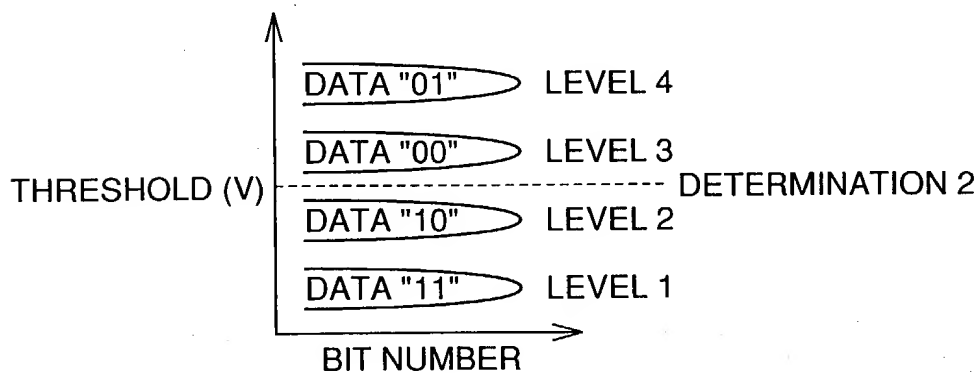


FIG.20

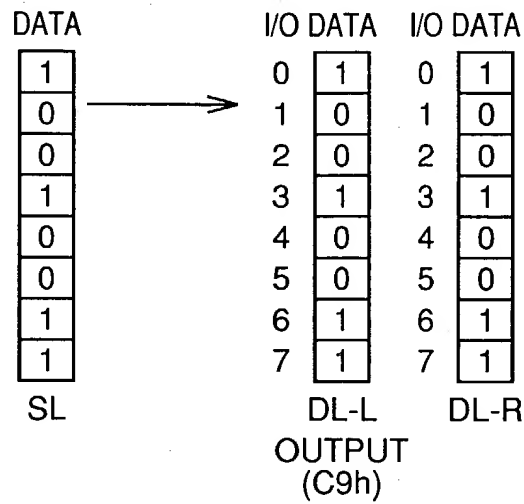


FIG.21

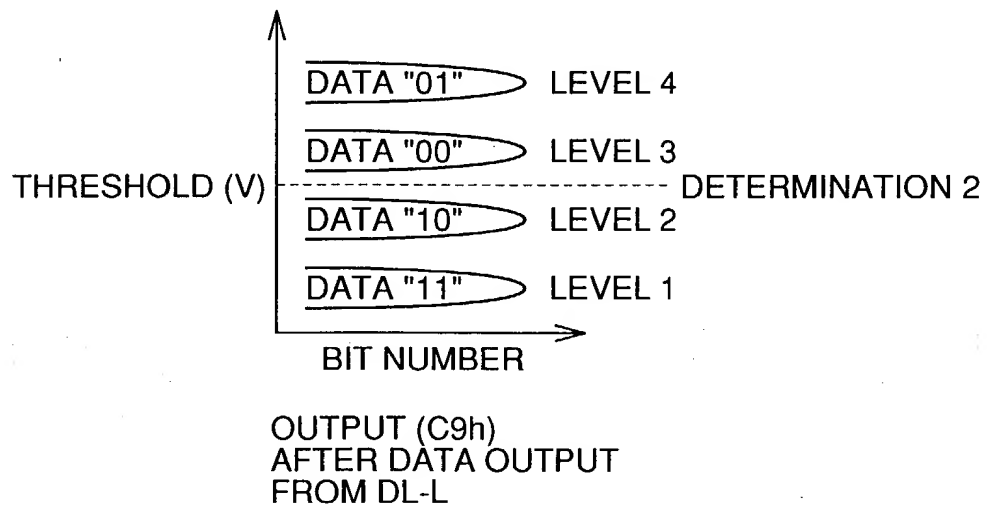


FIG.22

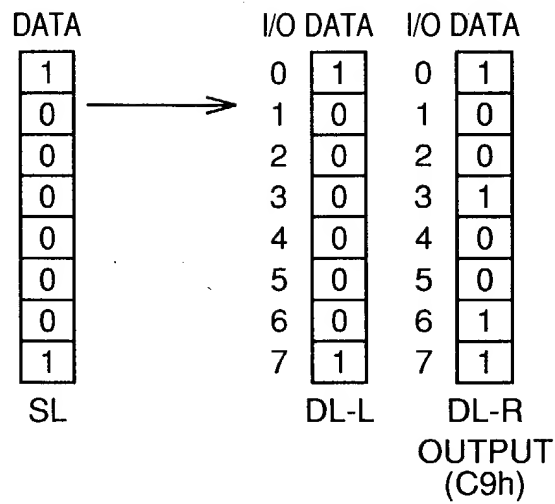


FIG.23

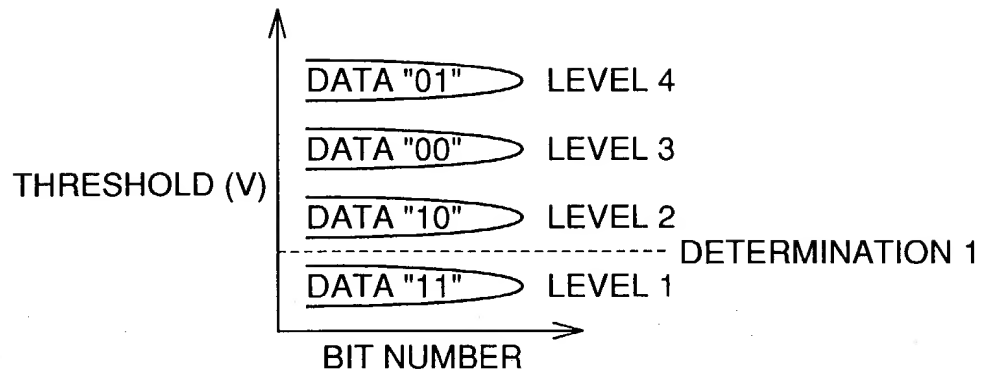


FIG.24

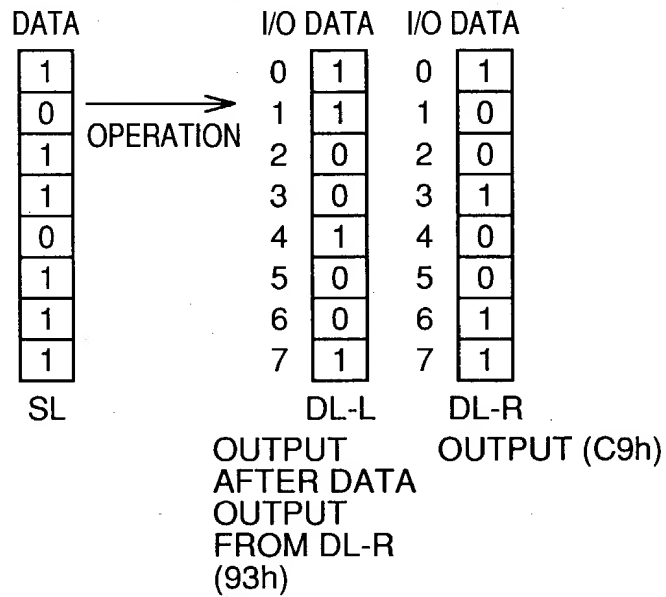


FIG.25

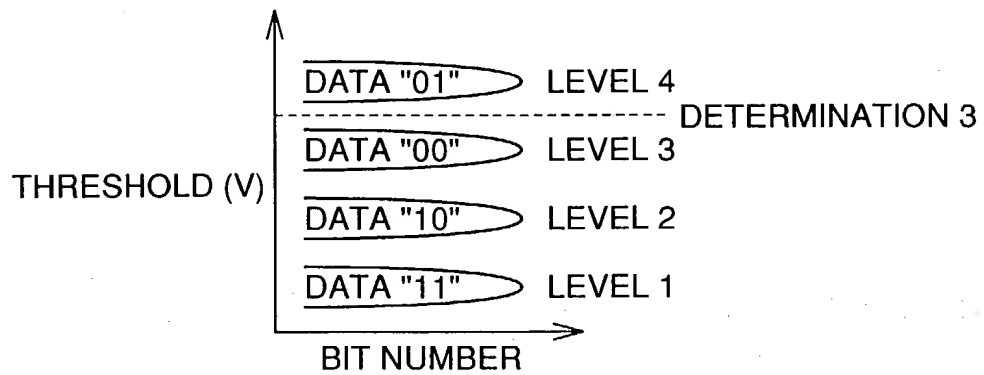


FIG.26

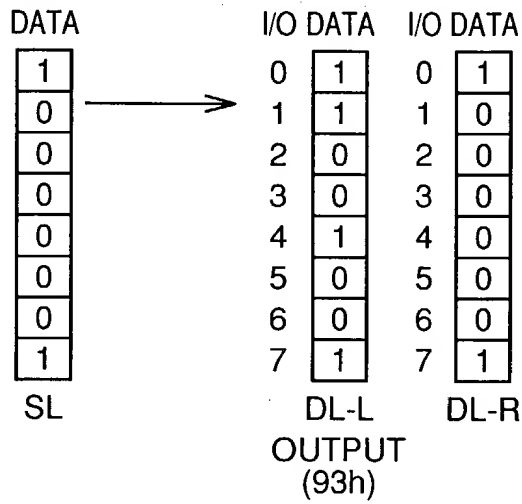


FIG.27

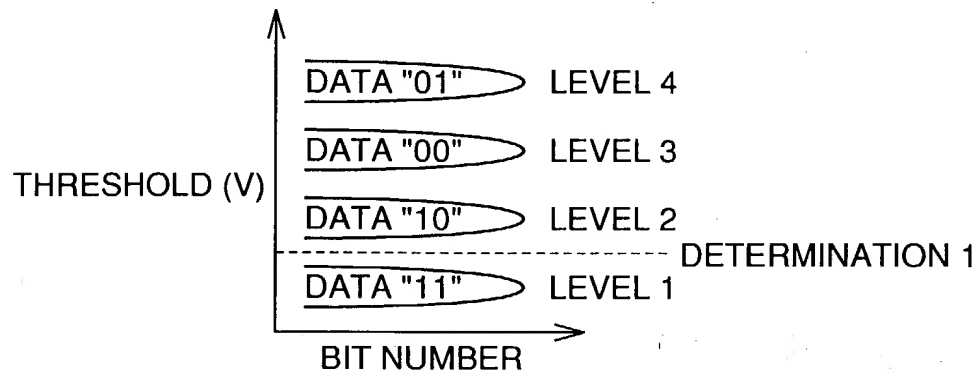


FIG.28

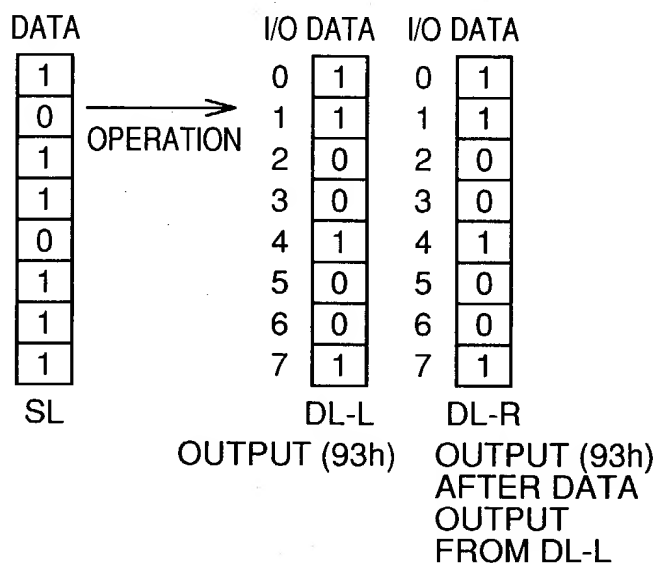


FIG.29

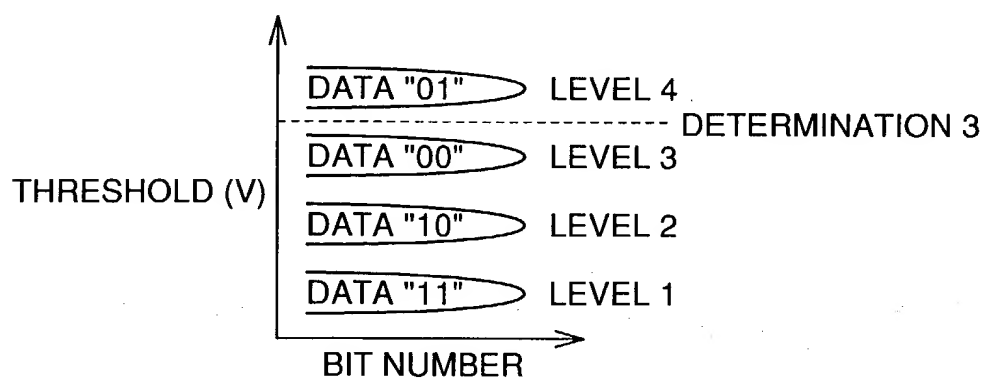


FIG.30

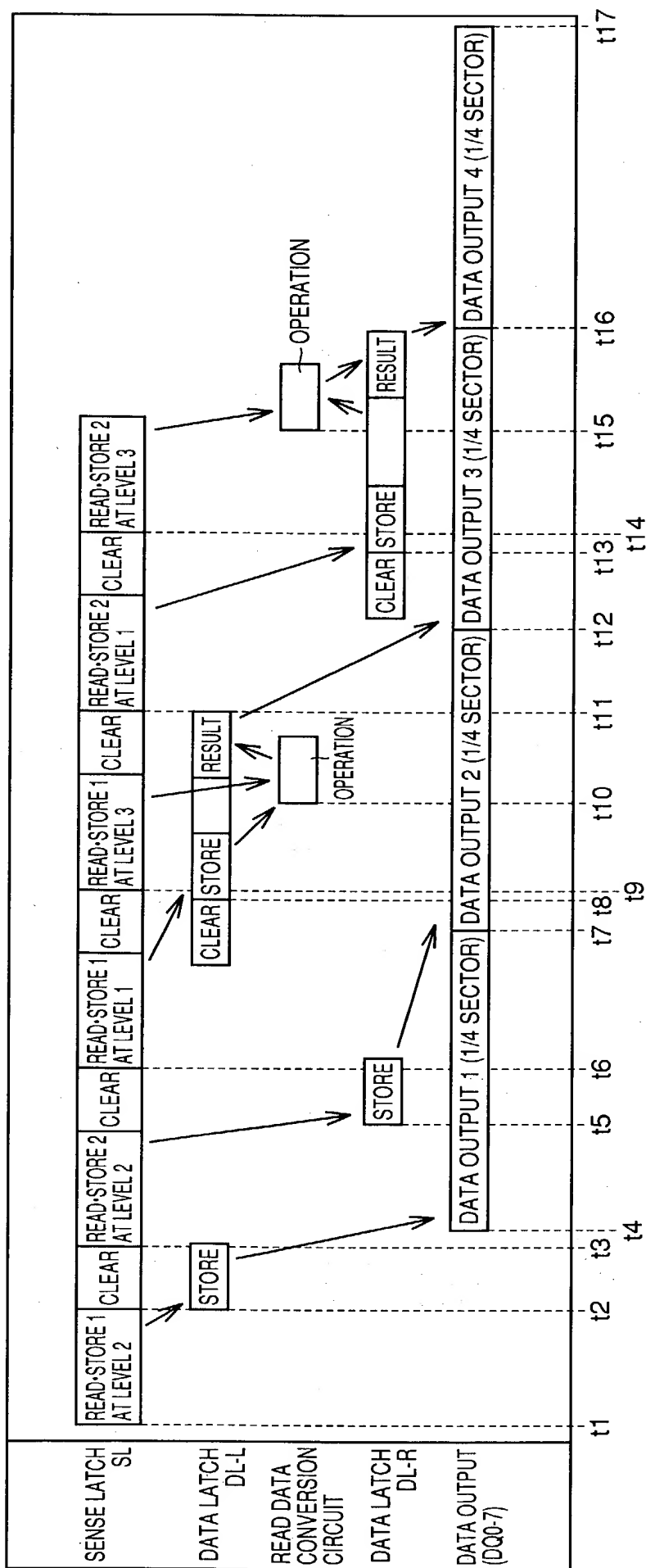


FIG.31

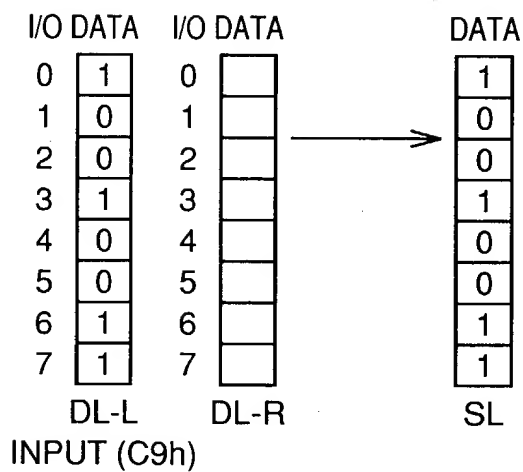


FIG.32

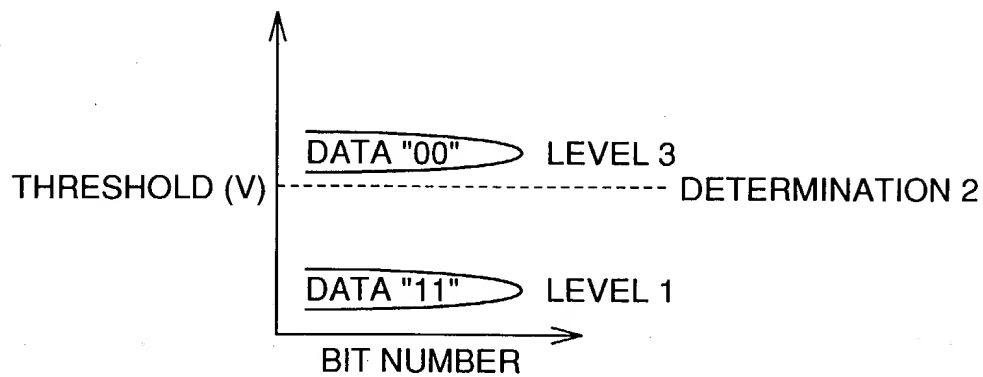


FIG.33

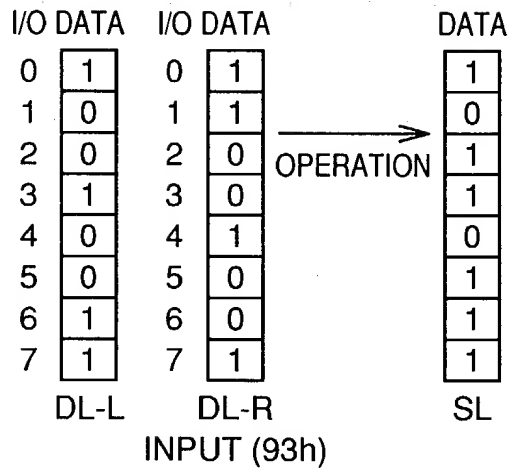


FIG.34

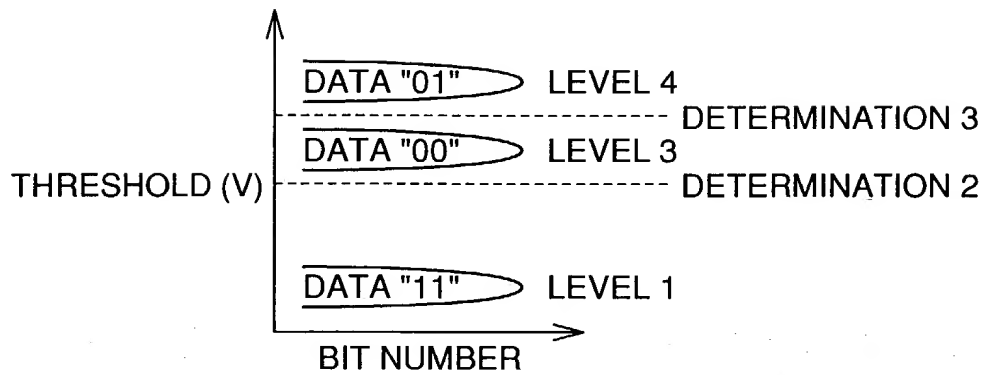


FIG.35

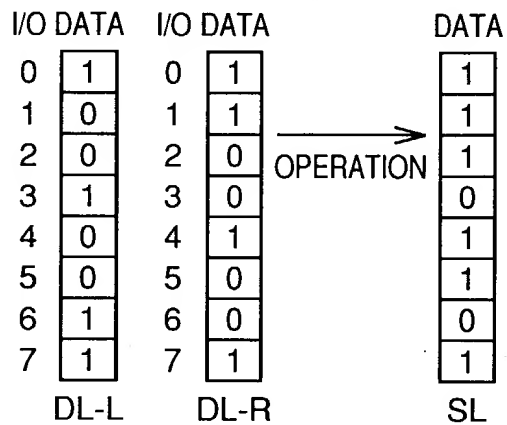


FIG.36

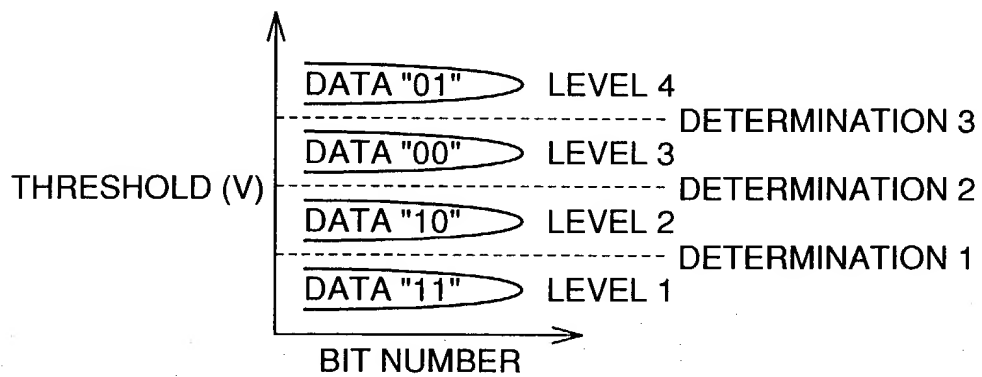




FIG.38

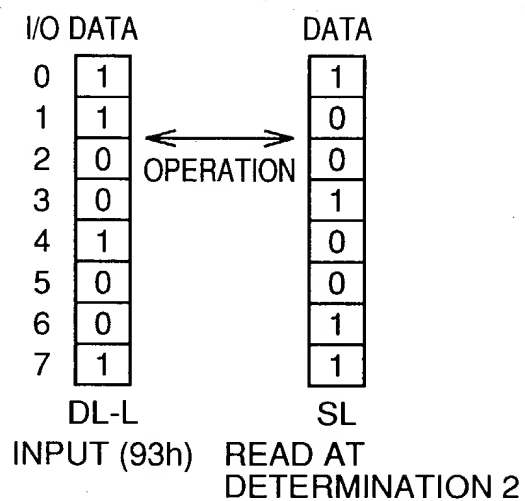


FIG.39

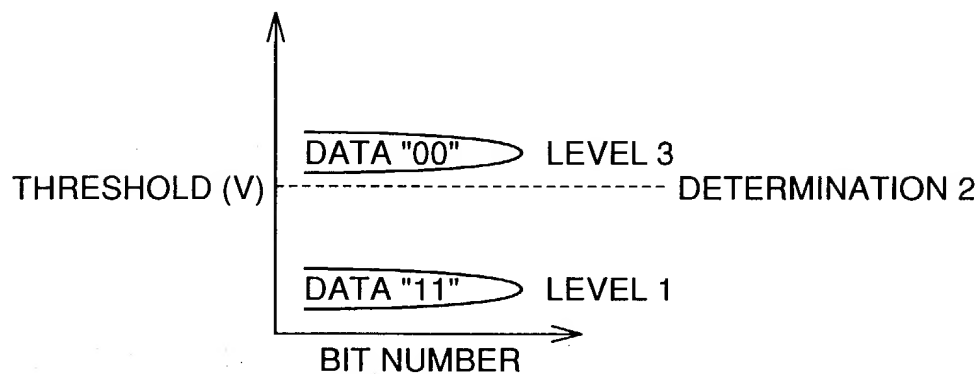


FIG.40

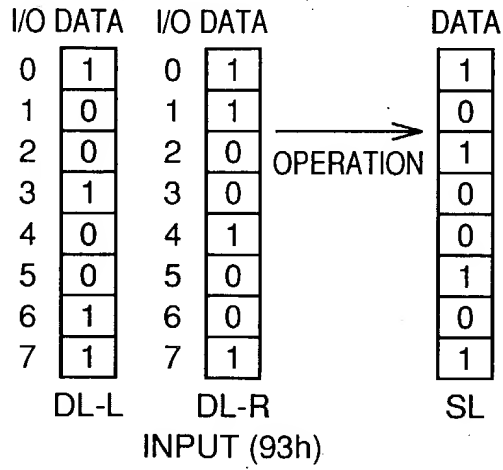


FIG.41

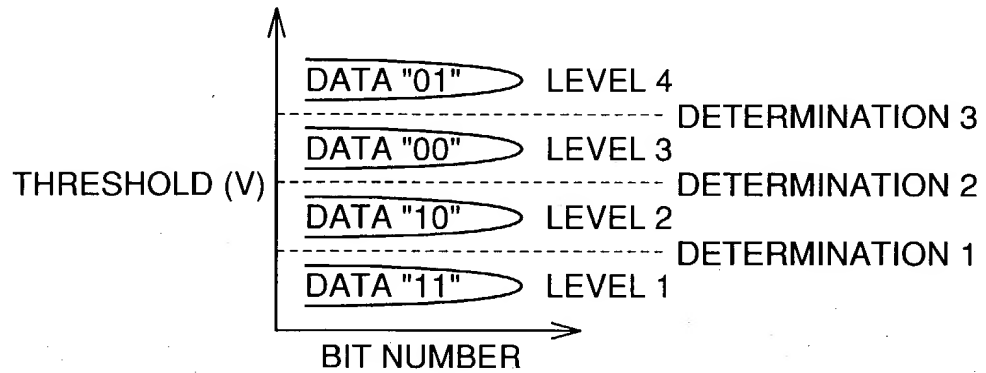
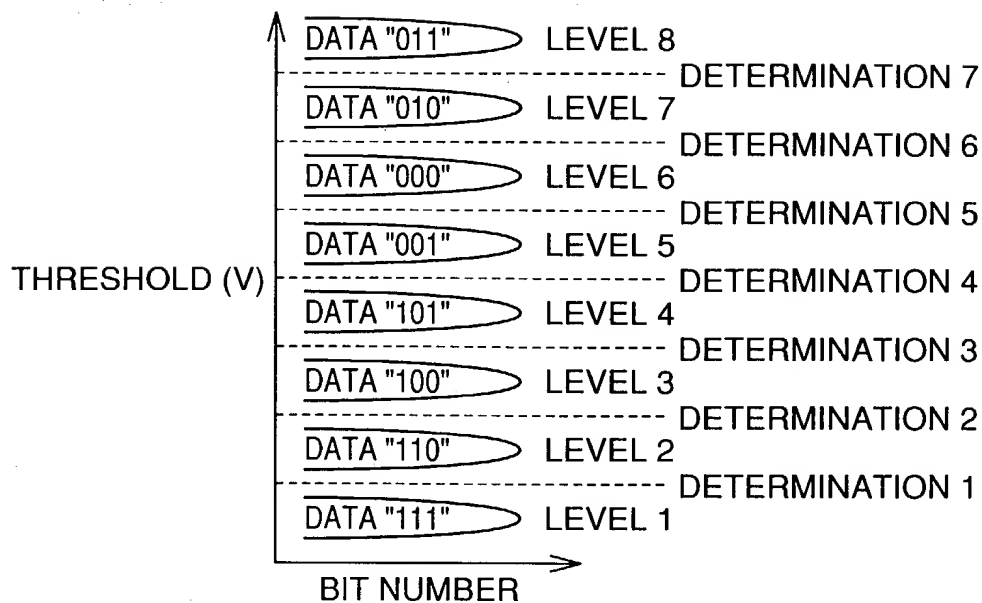




FIG.42

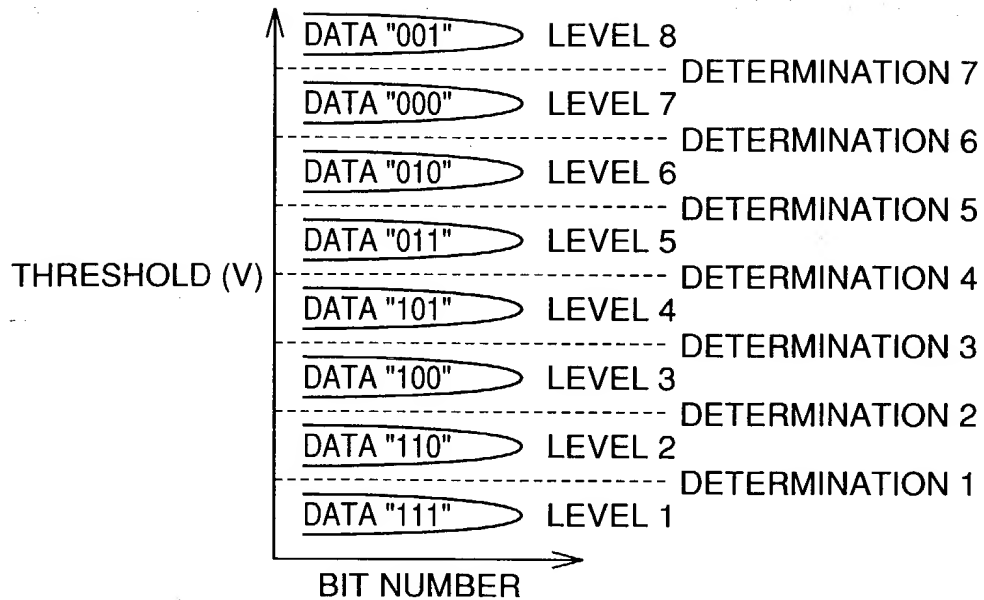


MOST SIGNIFICANT BIT DEFINED
AT DETERMINATION 4
INTERMEDIATE BIT DEFINED
AT DETERMINATION 2 & 6
LEAST SIGNIFICANT BIT DEFINED
AT DETERMINATION 1, 3, 5 & 7

OK



FIG.43



MOST SIGNIFICANT BIT DEFINED
AT DETERMINATION 4
"0" & "1" AT LEVELS 3, 4, 5 & 6
AT DETERMINATION 2 & 6
NOT DEFINED
LEAST SIGNIFICANT BIT DEFINED
AT DETERMINATION 1, 3, 5 & 7

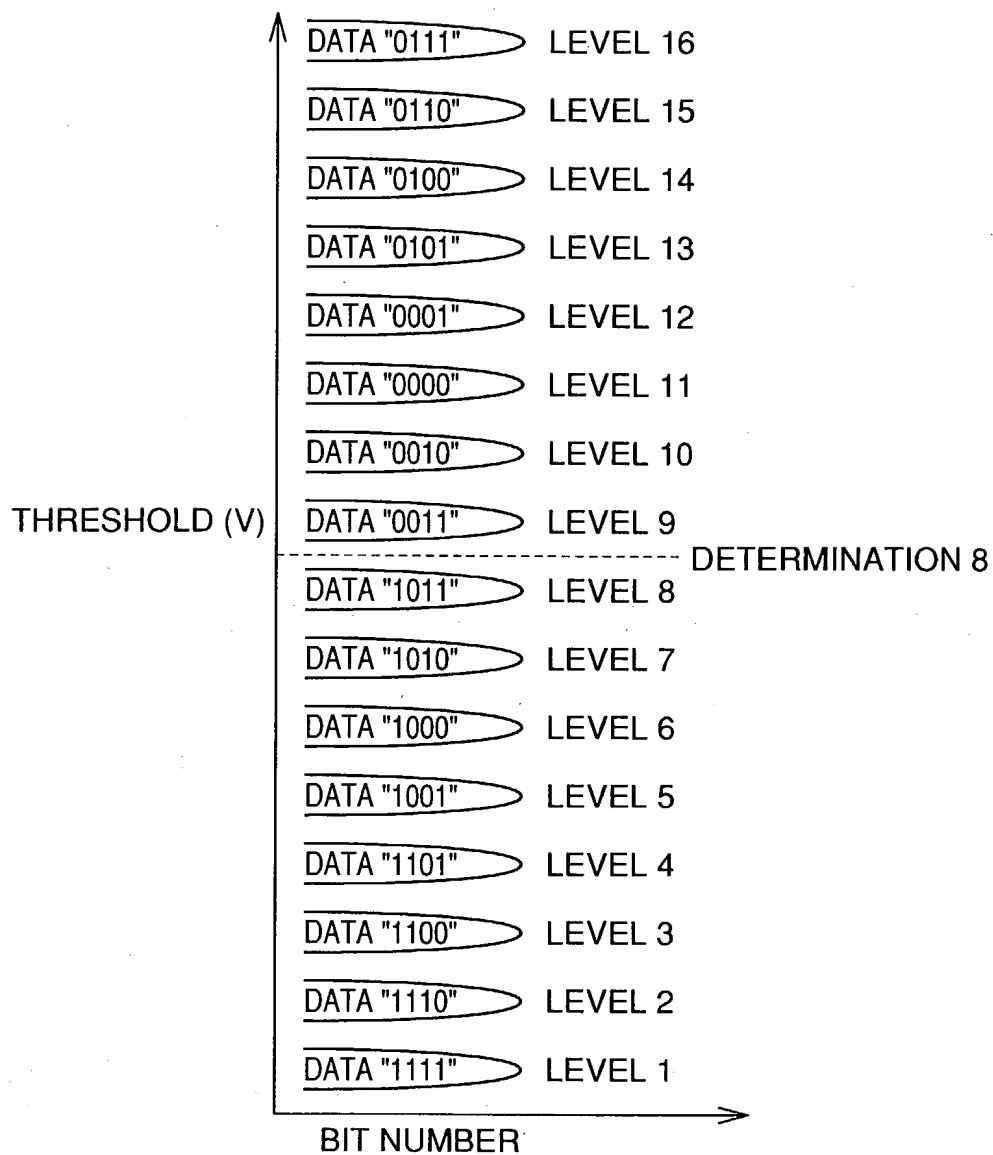
NG

FIG.44

	IN-CELL DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
MC0	"0111" 0	→	0 0	0	0	0
MC1	"0110" 0		1 0	1	1	1
MC2	"0100" 0		2 0	2	2	2
MC3	"0101" 0		3 0	3	3	3
MC4	"0001" 0		4 0	4	4	4
MC5	"0000" 0		5 0	5	5	5
MC6	"0010" 0		6 0	6	6	6
MC7	"0011" 0		7 0	7	7	7
MC8	"1011" 1		0 1	0	0	0
MC9	"1010" 1		1 1	1	1	1
MC10	"1000" 1		2 1	2	2	2
MC11	"1001" 1		3 1	3	3	3
MC12	"1101" 1		4 1	4	4	4
MC13	"1100" 1		5 1	5	5	5
MC14	"1110" 1		6 1	6	6	6
MC15	"1111" 1		7 1	7	7	7
	SL		DL-1	DL-2	DL-3	DL-4
			OUTPUT (00h-FFh)			



FIG.45



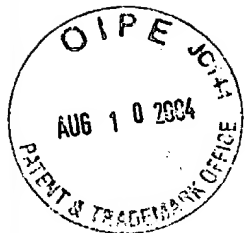


FIG.46

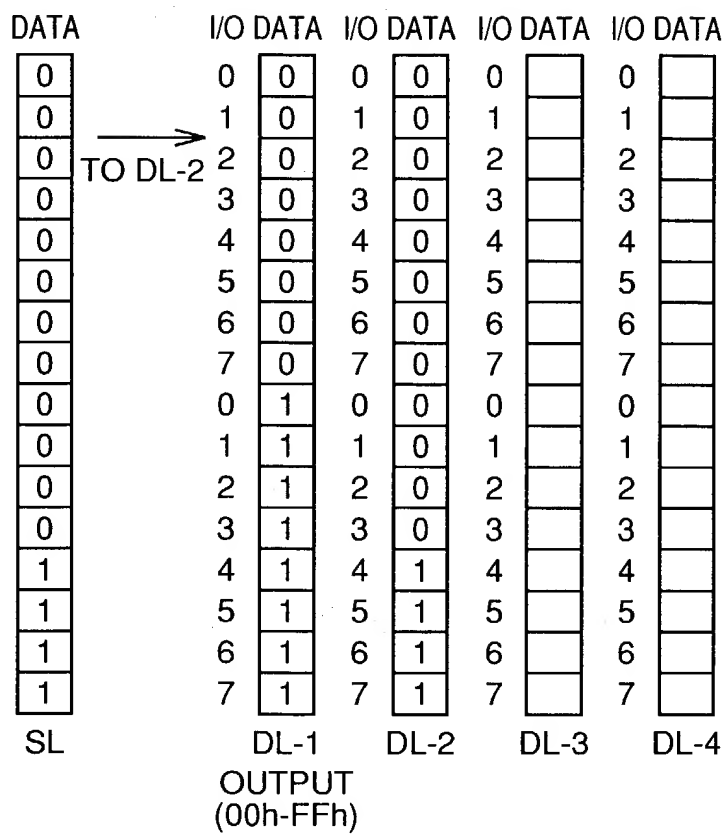




FIG.47

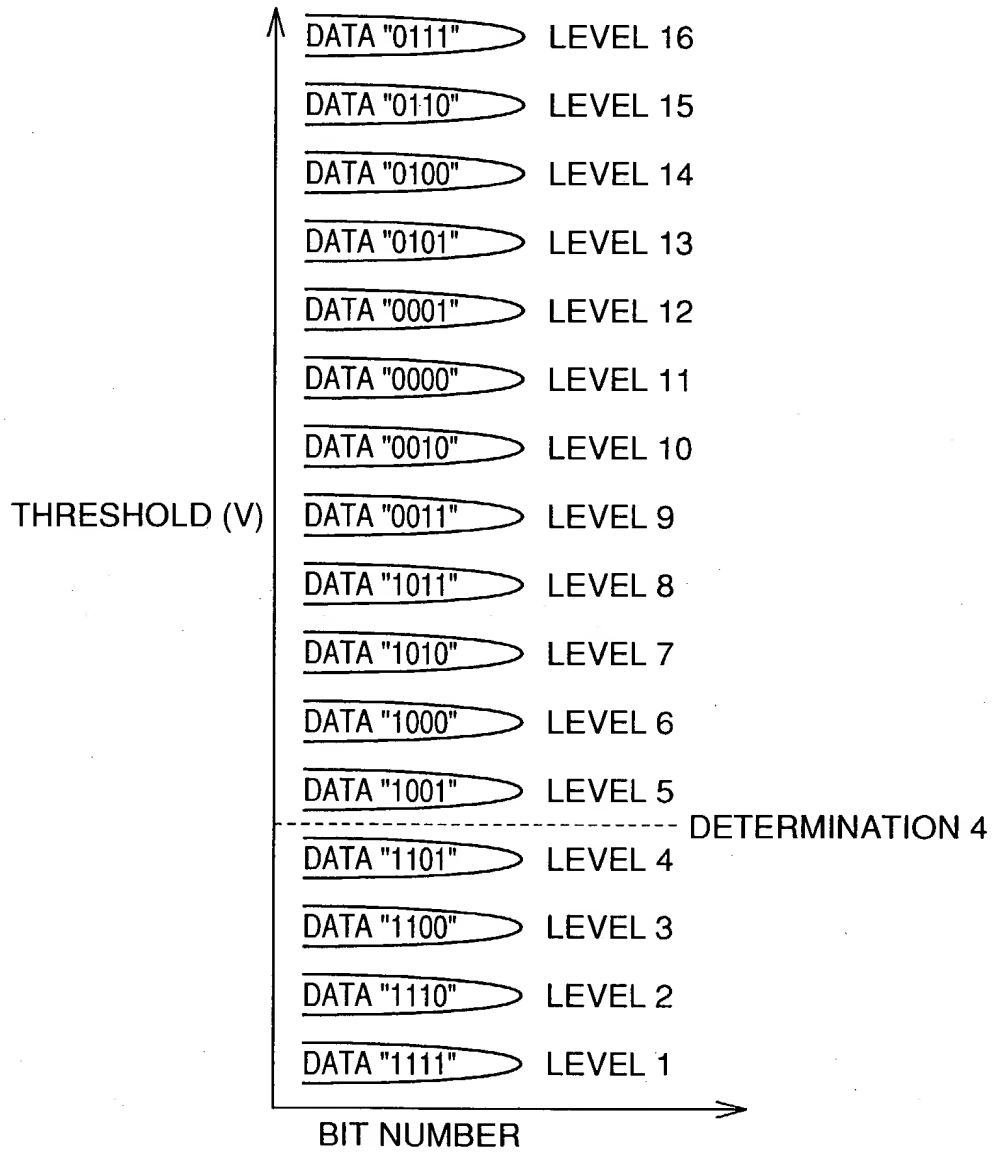


FIG.48

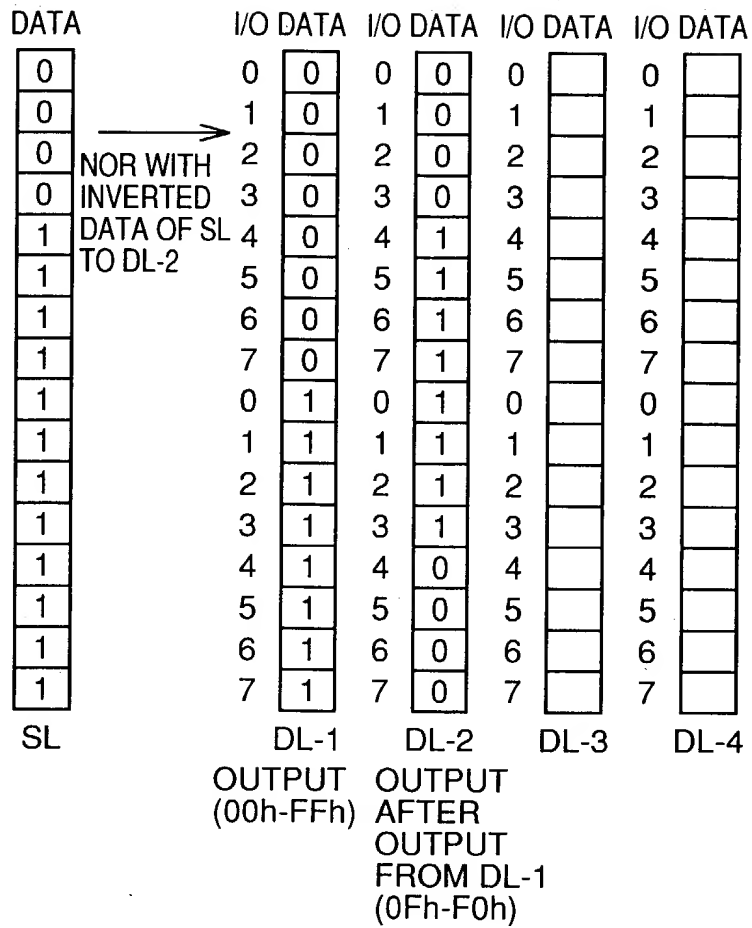




FIG.49

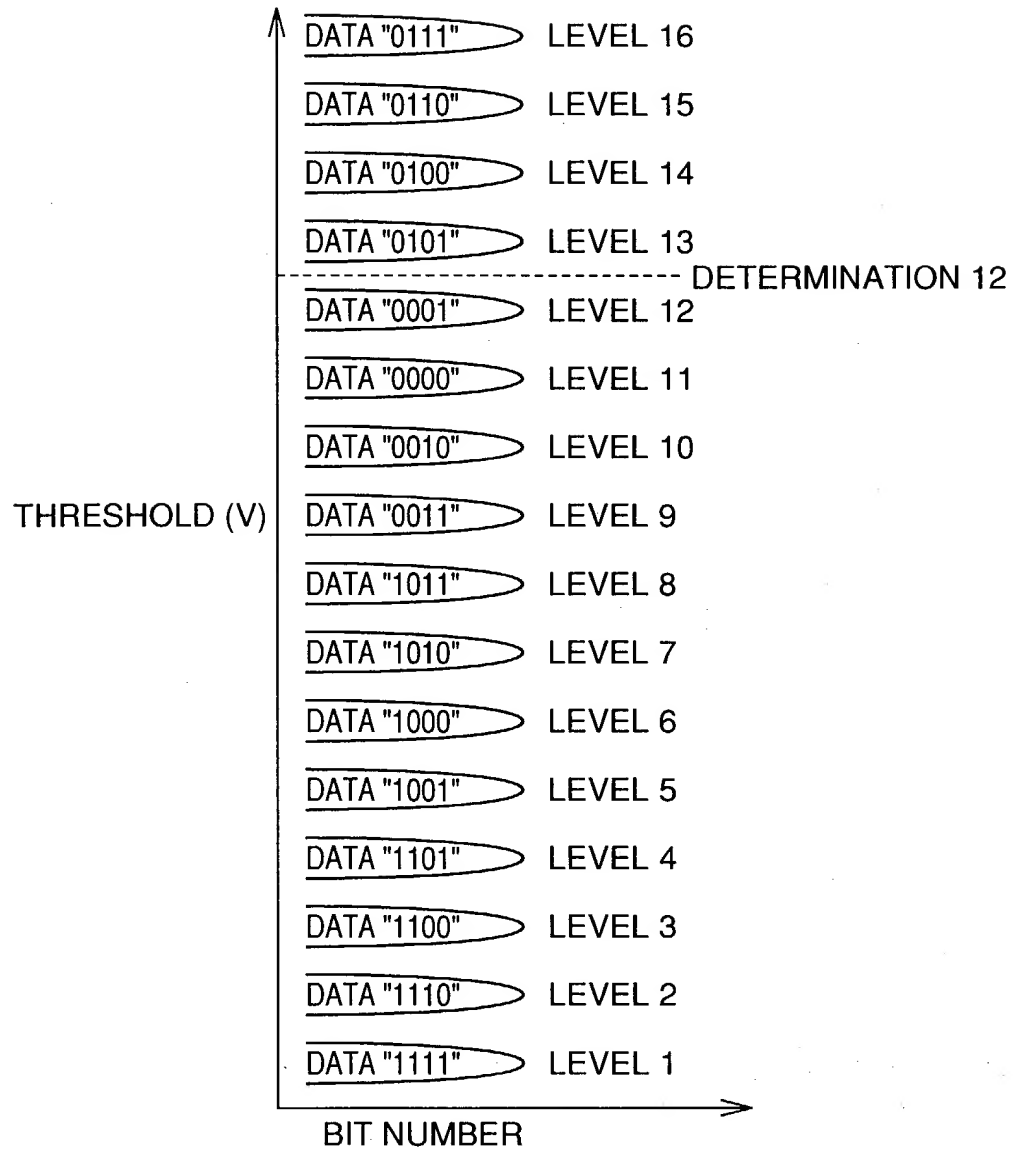


FIG.50

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0	→ TO DL-3	2	0	2	0
0		3	0	3	0
0		4	0	4	1
0		5	0	5	1
0		6	0	6	1
0		7	0	7	1
0		0	1	0	0
0		1	1	1	0
0		2	1	2	0
0		3	1	3	0
0		4	1	4	0
0		5	1	5	0
1		6	1	6	1
1		7	1	7	1
SL		DL-1	DL-2	DL-3	DL-4
		OUTPUT	OUTPUT		
		(00h-FFh)	AFTER		
			OUTPUT		
			FROM DL-1		
			(0Fh-F0h)		



FIG.51

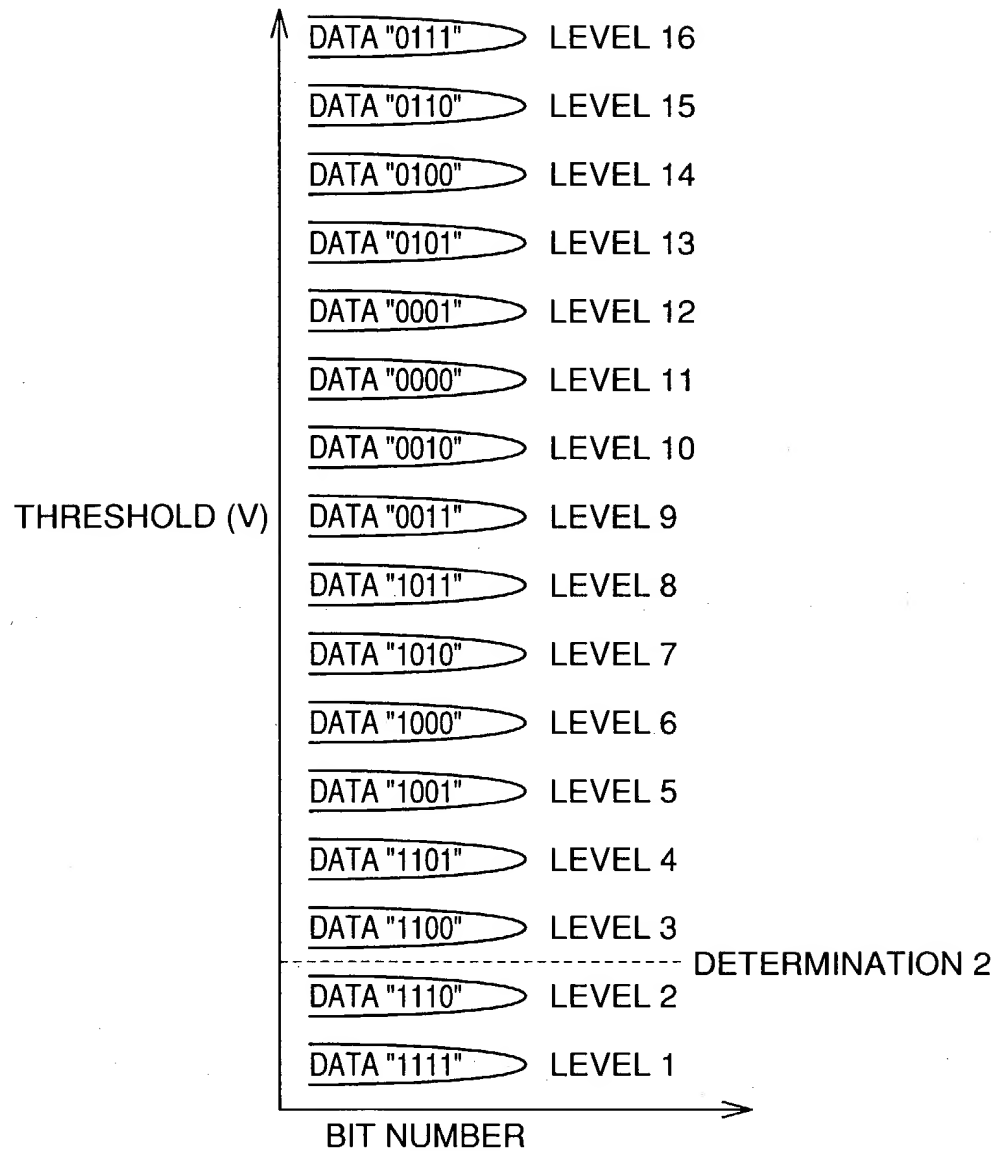




FIG.53

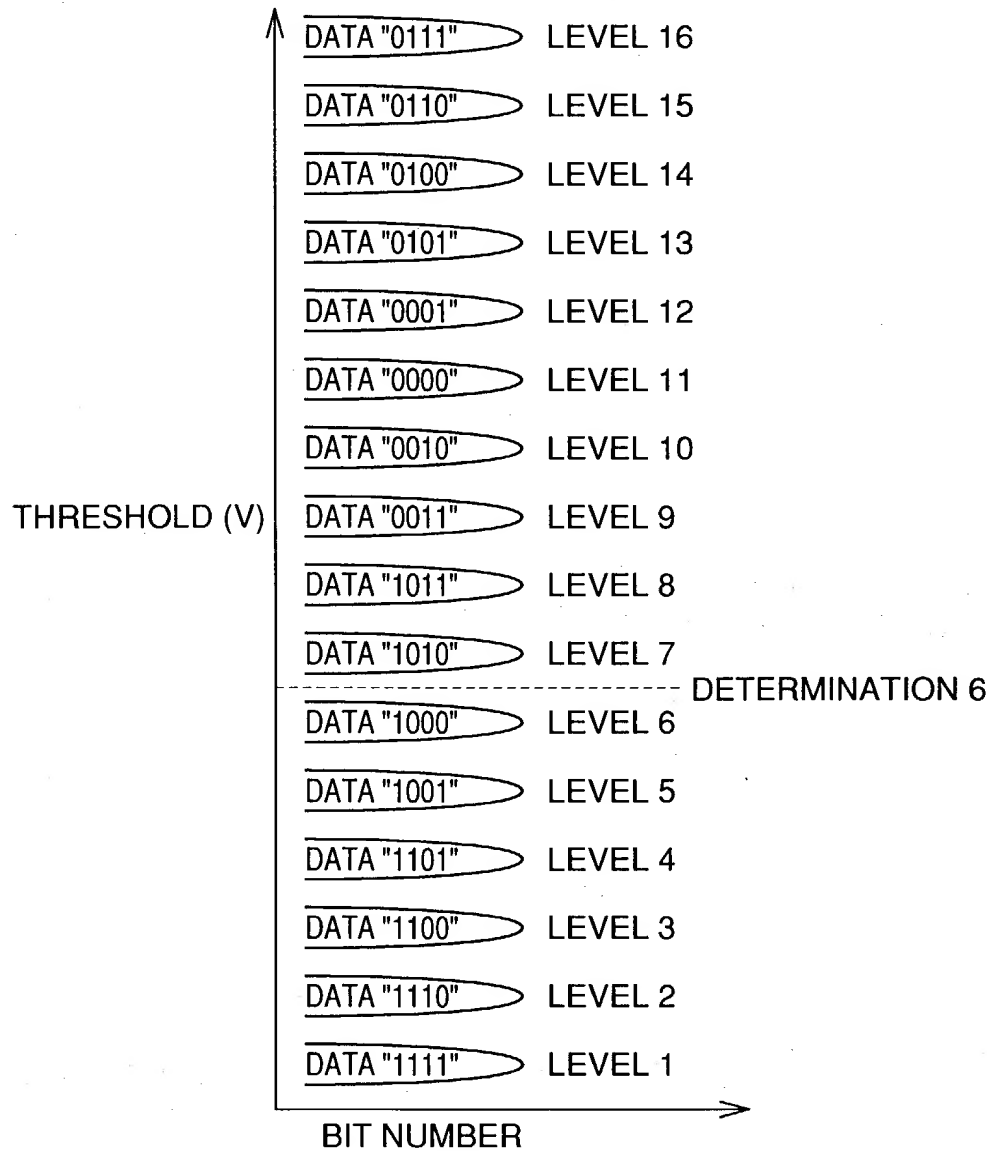


FIG.54

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0	→ TO DL-4	2	0	2	0
0		3	0	3	0
0		4	0	4	0
0		5	0	5	0
1		6	0	6	1
1		7	0	7	1
1		0	1	0	0
1		1	1	1	0
1		2	1	2	1
1		3	1	3	1
1		4	1	4	1
1		5	1	5	1
1		6	1	6	0
1		7	1	7	0
SL		DL-1	DL-2	DL-3	DL-4
		OUTPUT	OUTPUT		
		(00h-FFh)	AFTER		
			OUTPUT		
			FROM DL-1		
			(0Fh-F0h)		



FIG.55

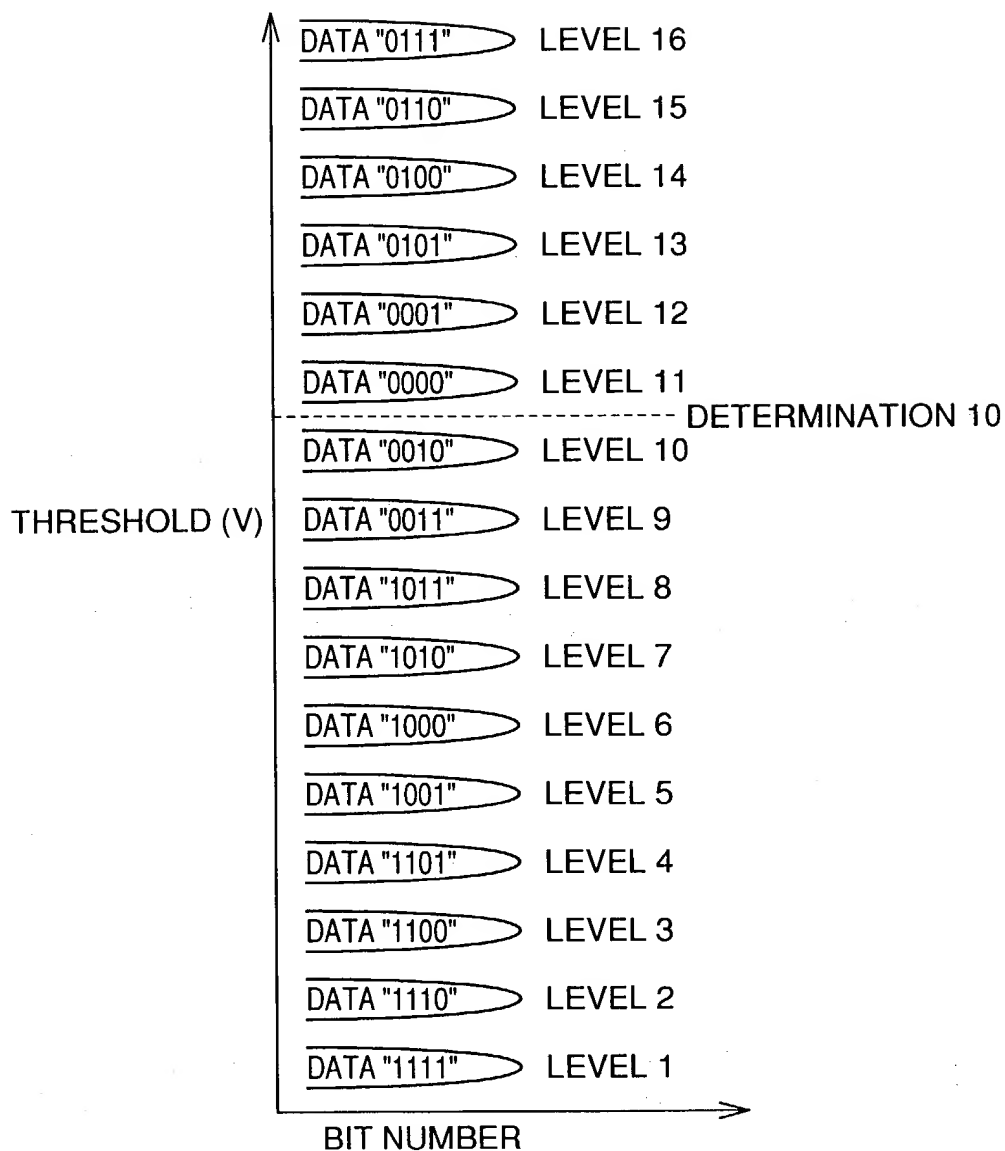


FIG.56

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0 0	0 0	0 0	0 0
0		1 0	1 0	1 0	1 0
1		2 0	2 0	2 0	2 1
1	NOR	3 0	3 0	3 0	3 1
1	INVERTED	4 0	4 1	4 0	4 1
1	DATA OF SL	5 0	5 1	5 0	5 1
1	AND DATA	6 0	6 1	6 0	6 0
1	OF DL-4	7 0	7 1	7 0	7 0
1	TO DL-4	0 1	0 1	0 0	0 0
1		1 1	1 1	1 0	1 0
1		2 1	2 1	2 1	2 0
1		3 1	3 1	3 1	3 0
1		4 1	4 0	4 1	4 0
1		5 1	5 0	5 1	5 0
1		6 1	6 0	6 0	6 0
1		7 1	7 0	7 0	7 0
SL		DL-1	DL-2	DL-3	DL-4
		OUTPUT	OUTPUT		
		(00h-FFh)	AFTER		
			OUTPUT		
			FROM DL-1		
			(0Fh-F0h)		



FIG.57

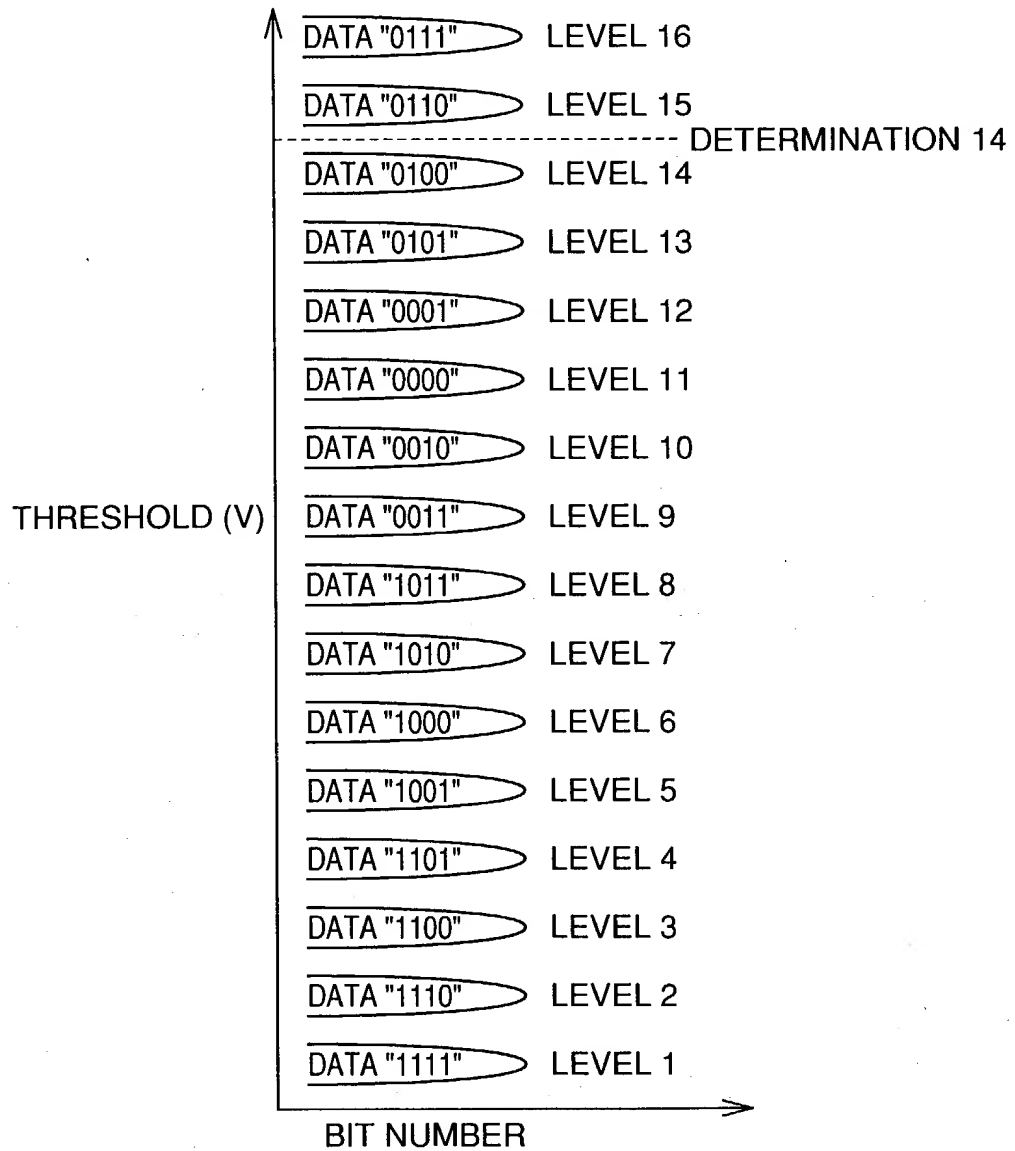




FIG.58

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
	0 0	0 0	0 0	0
	1 0	1 0	1 0	1
	2 0	2 0	2 1	2
	3 0	3 0	3 1	3
	4 0	4 1	4 1	4
	5 0	5 1	5 1	5
	6 0	6 1	6 0	6
	7 0	7 1	7 0	7
	0 1	0 1	0 0	0
	1 1	1 1	1 0	1
	2 1	2 1	2 1	2
	3 1	3 1	3 1	3
	4 1	4 0	4 1	4
	5 1	5 0	5 1	5
	6 1	6 0	6 0	6
	7 1	7 0	7 0	7
SL	DL-1	DL-2	DL-3	DL-4
	OUTPUT (00h-FFh)	OUTPUT AFTER OUTPUT FROM DL-1 (0Fh-F0h)	OR DATA OF DL-3 AND DL-4 AND STORE RESULT IN DL-3	



FIG.59

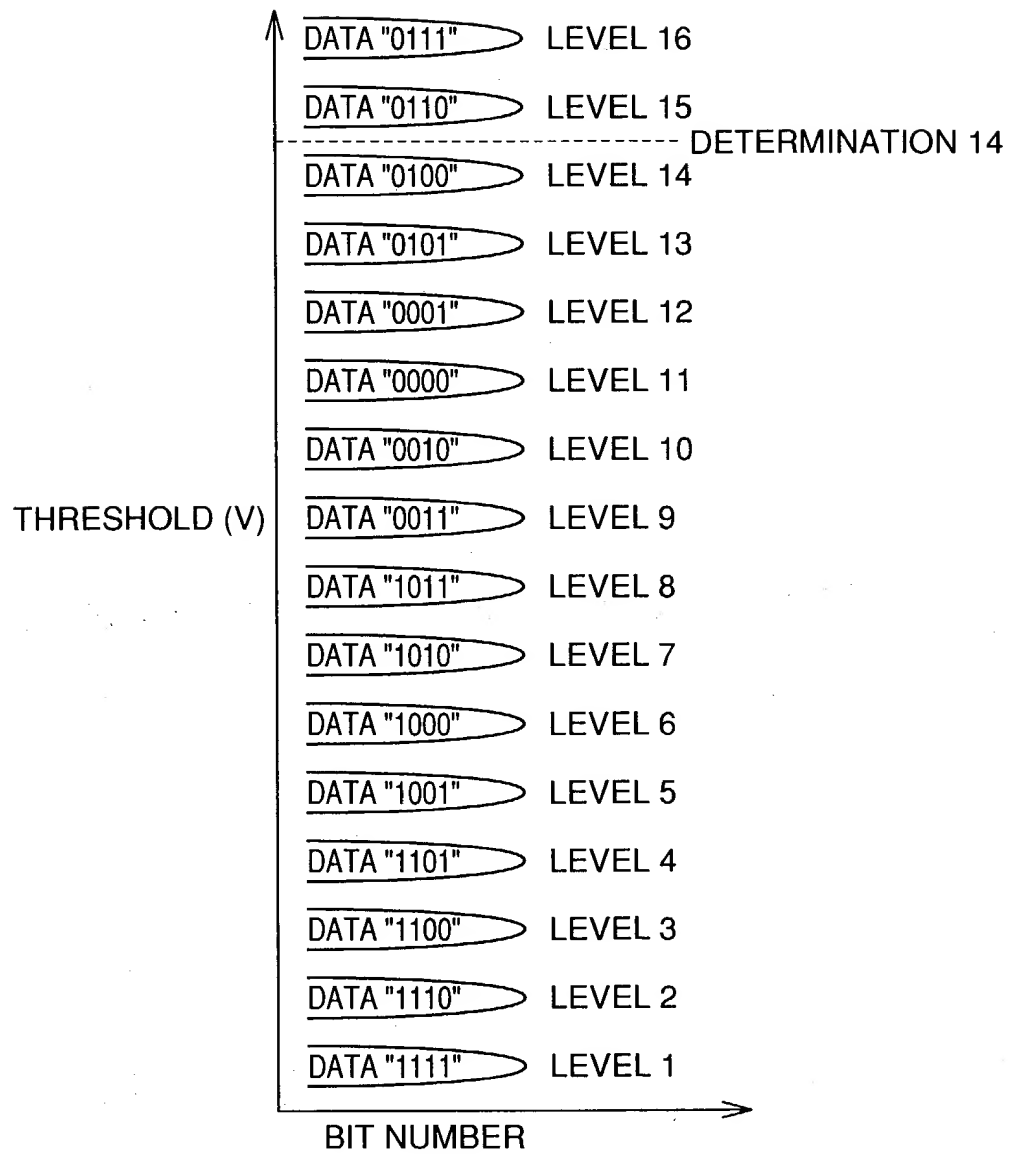


FIG.60

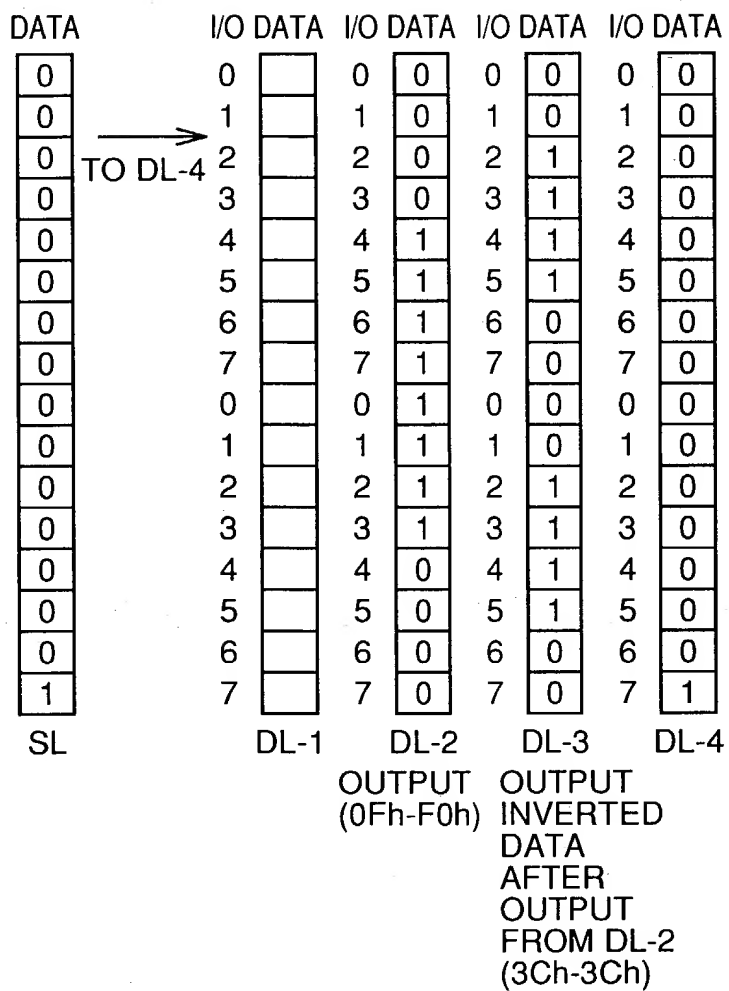


FIG.61

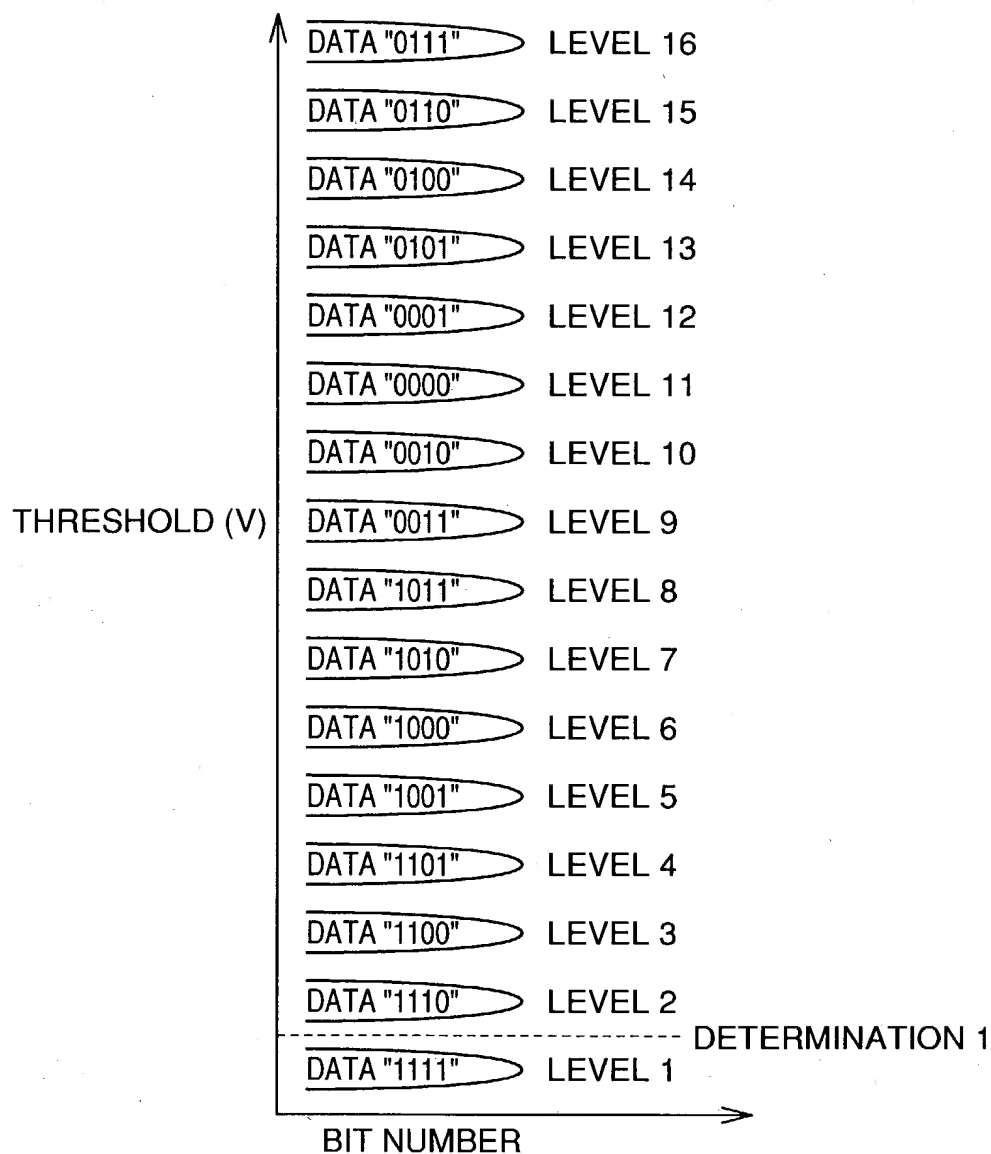


FIG.62

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0		2	0	2	1
0	NOR	3	0	3	1
0	INVERTED	4	1	4	1
0	DATA OF SL	5	1	5	1
0	AND DATA	6	1	6	0
0	OF DL-4	7	1	7	0
0	TO DL-4	0	1	0	0
0		1	1	1	0
0		2	1	2	1
0		3	1	3	1
0		4	0	4	1
1		5	0	5	1
1		6	0	6	0
1		7	0	7	0
SL		DL-1	DL-2	DL-3	DL-4
			OUTPUT	OUTPUT	
			(00h-FFh)	INVERTED	
				DATA	
				AFTER	
				OUTPUT	
				FROM DL-2	
				(00h-FFh)	



FIG.63

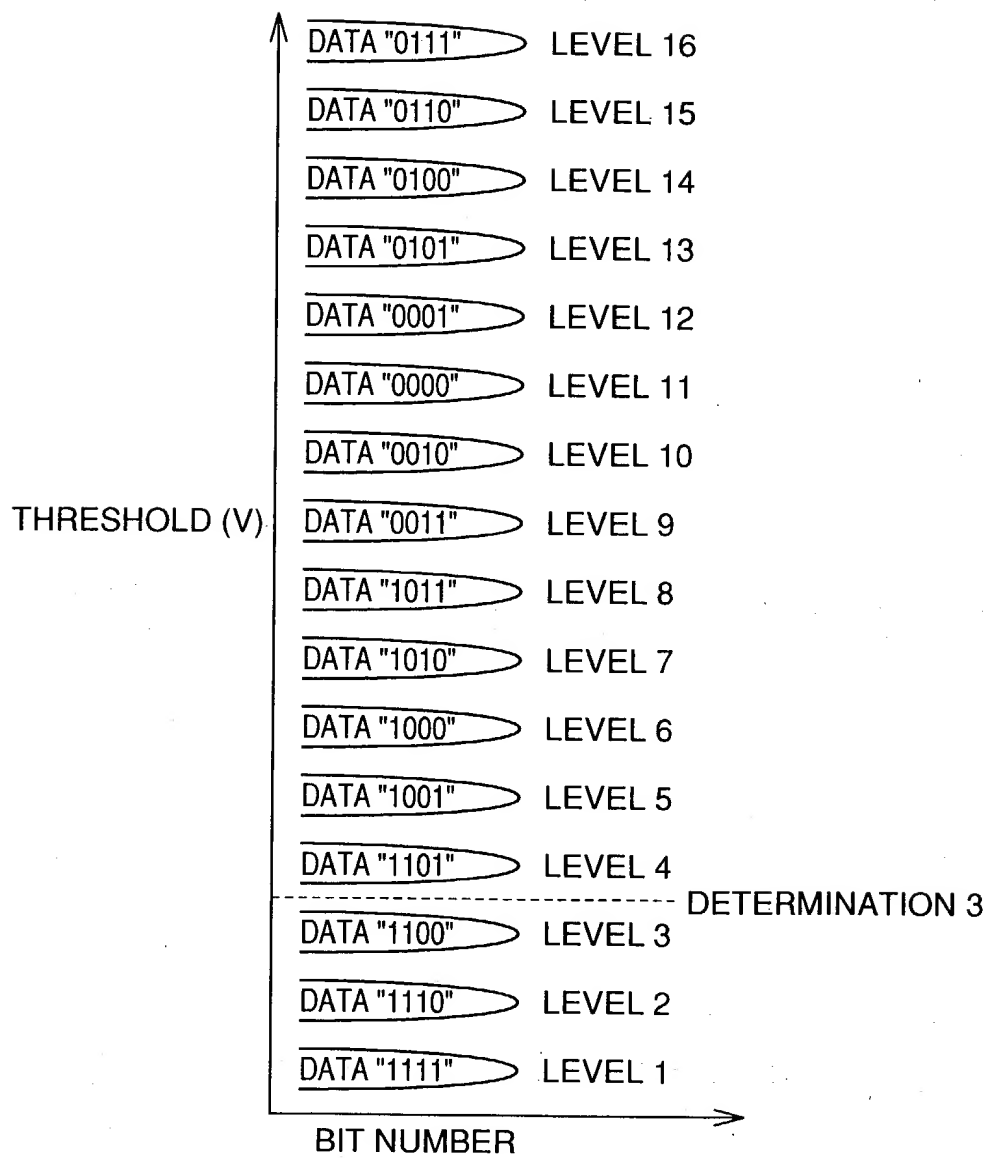


FIG.64

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0	→ TO DL-1	2	0	2	1
0		3	0	3	1
0		4	0	4	1
0		5	0	5	1
0		6	0	6	0
0		7	0	7	0
0		0	0	0	0
0		1	0	1	0
0		2	0	2	1
1		3	1	3	1
1		4	1	4	1
1		5	1	5	0
1		6	1	6	0
1		7	1	7	0
SL		DL-1	DL-2	DL-3	DL-4
		OUTPUT (0Fh-F0h)		OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)	



FIG.65

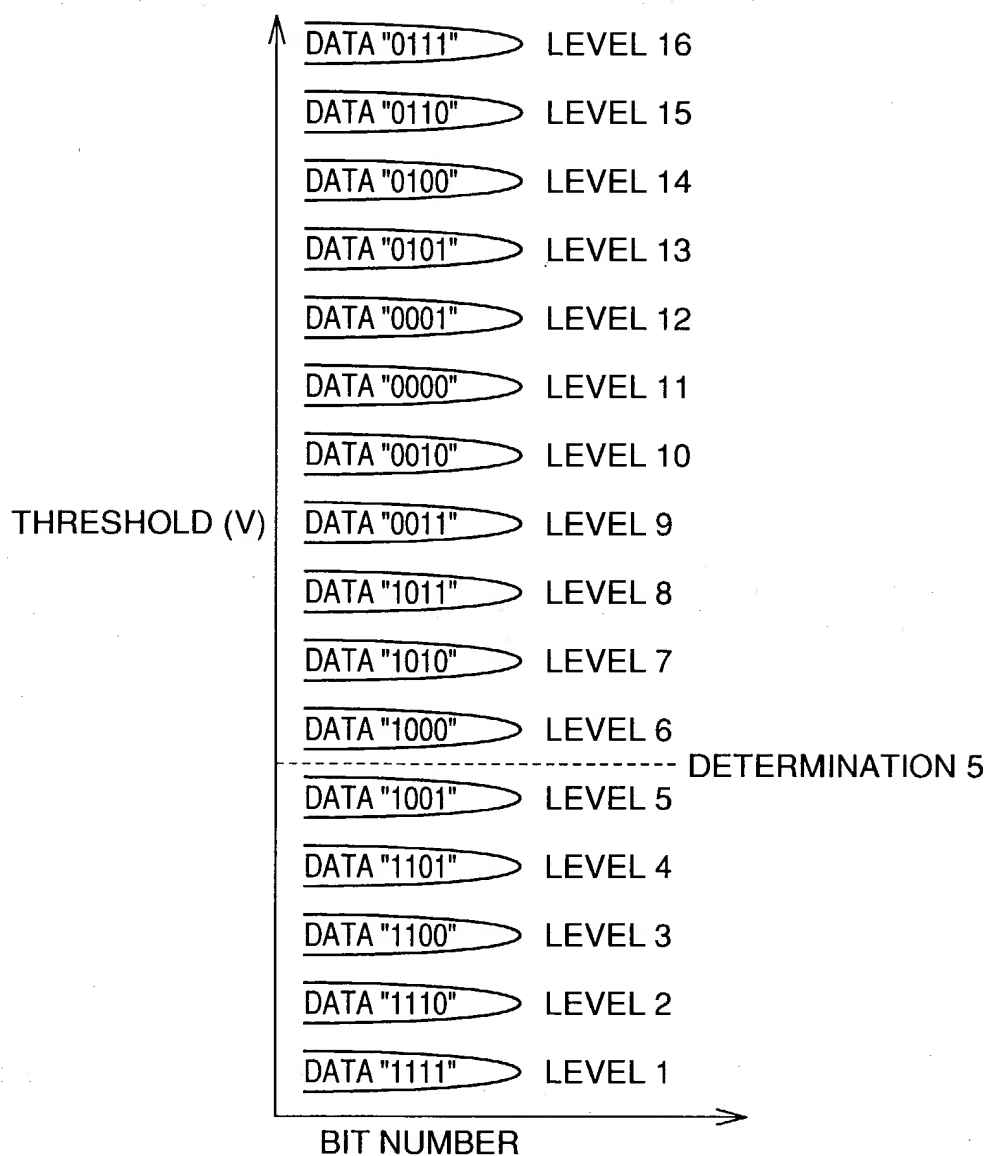




FIG.66

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0		2	0	2	1
0	NOR	3	0	3	1
0	INVERTED	4	0	4	1
0	DATA OF SL	5	0	5	1
0	AND DATA	6	0	6	0
0	OF DL-1	7	0	7	0
0	TO DL-1	0	0	0	0
0		1	1	1	0
1		2	1	2	1
1		3	0	3	1
1		4	0	4	1
1		5	0	5	1
1		6	0	6	0
1		7	0	7	0
SL		DL-1	DL-2	DL-3	DL-4
		OUTPUT	OUTPUT		
		(00h-FFh)	INVERTED		
			DATA		
			AFTER		
			OUTPUT		
			FROM DL-2		
			(00h-FFh)		



FIG.67

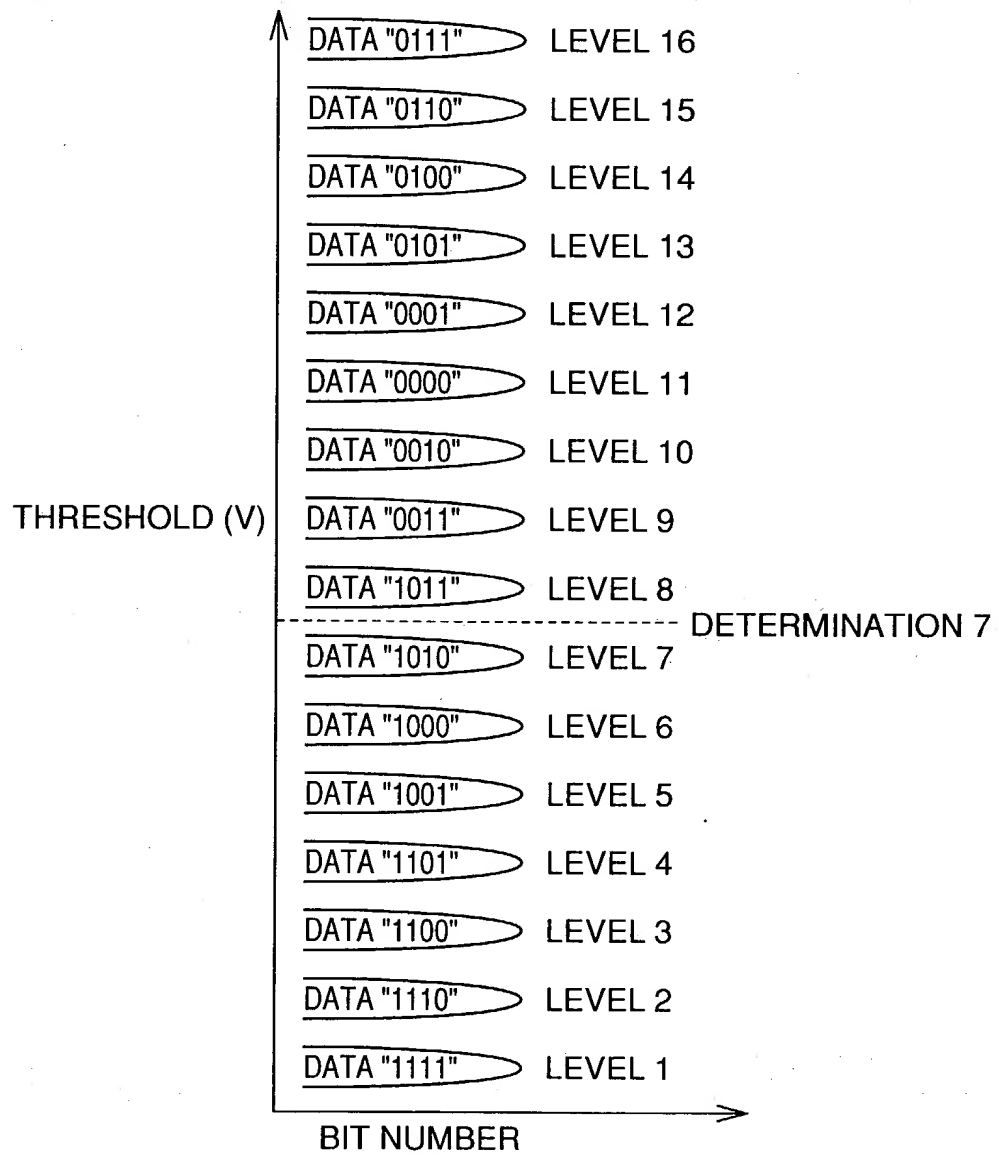


FIG.68

		OR DATA OF DL-1 AND DL-4 TO DL-4							
DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
SL		0	0	0	0	0	0	0	0
		1	0	1	0	1	0	1	0
		2	0	2	0	2	1	2	0
		3	0	3	0	3	1	3	0
		4	0	4	1	4	1	4	0
		5	0	5	1	5	1	5	0
		6	0	6	1	6	0	6	0
		7	0	7	1	7	0	7	0
		0	0	0	1	0	0	0	0
		1	1	1	1	1	0	1	1
		2	1	2	1	2	1	2	1
		3	0	3	1	3	1	3	0
		4	0	4	0	4	1	4	0
		5	0	5	0	5	1	5	1
		6	0	6	0	6	0	6	1
		7	0	7	0	7	0	7	0
		DL-1		DL-2		DL-3		DL-4	
		OUTPUT (0Fh-F0h)				OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)			



FIG.69

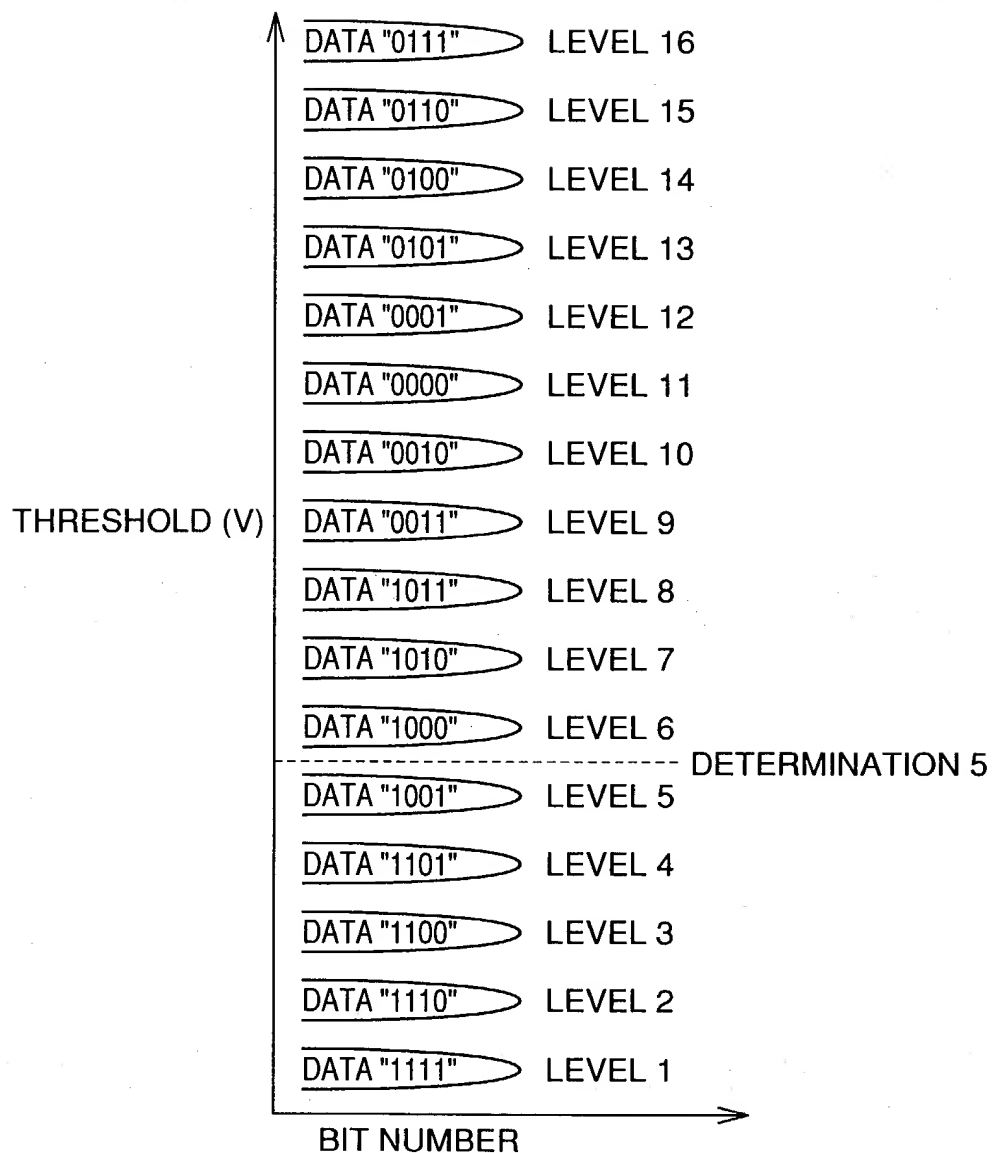


FIG.70

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0	→	2	0	2	1
0	TO DL-1	3	0	3	1
0		4	0	4	1
0		5	0	5	1
0		6	0	6	0
1		7	1	7	0
1		0	1	0	0
1		1	1	1	0
1		2	1	2	1
1		3	1	3	1
1		4	1	4	1
1		5	1	5	1
1		6	1	6	0
1		7	1	7	0
SL		DL-1	DL-2	DL-3	DL-4
		OUTPUT (00h-FFh)		OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)	



FIG.71

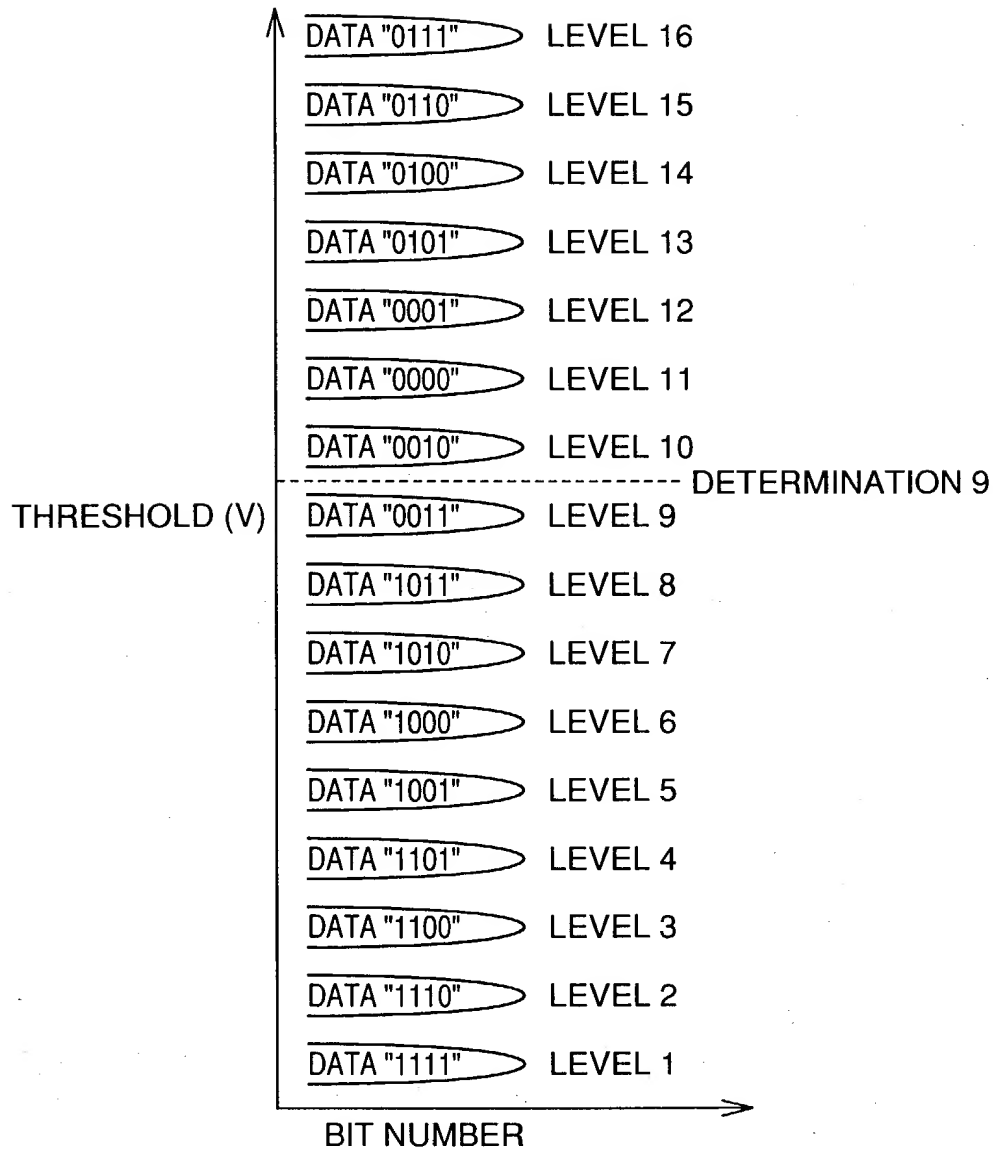


FIG.72

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0		2	0	2	1
0	NOR	3	0	3	1
0	INVERTED	4	0	4	1
1	DATA OF SL	5	1	5	1
1	AND DATA	6	1	6	0
1	OF DL-1	7	0	7	0
1	TO DL-1	0	0	0	0
1		1	0	1	0
1		2	0	2	1
1		3	0	3	1
1		4	0	4	1
1		5	0	5	1
1		6	0	6	0
1		7	0	7	0
1					
SL		DL-1	DL-2	DL-3	DL-4
			OUTPUT	OUTPUT	
			(00h-FFh)	INVERTED	
				DATA	
				AFTER	
				OUTPUT	
				FROM DL-2	
				(00h-FFh)	



FIG.73

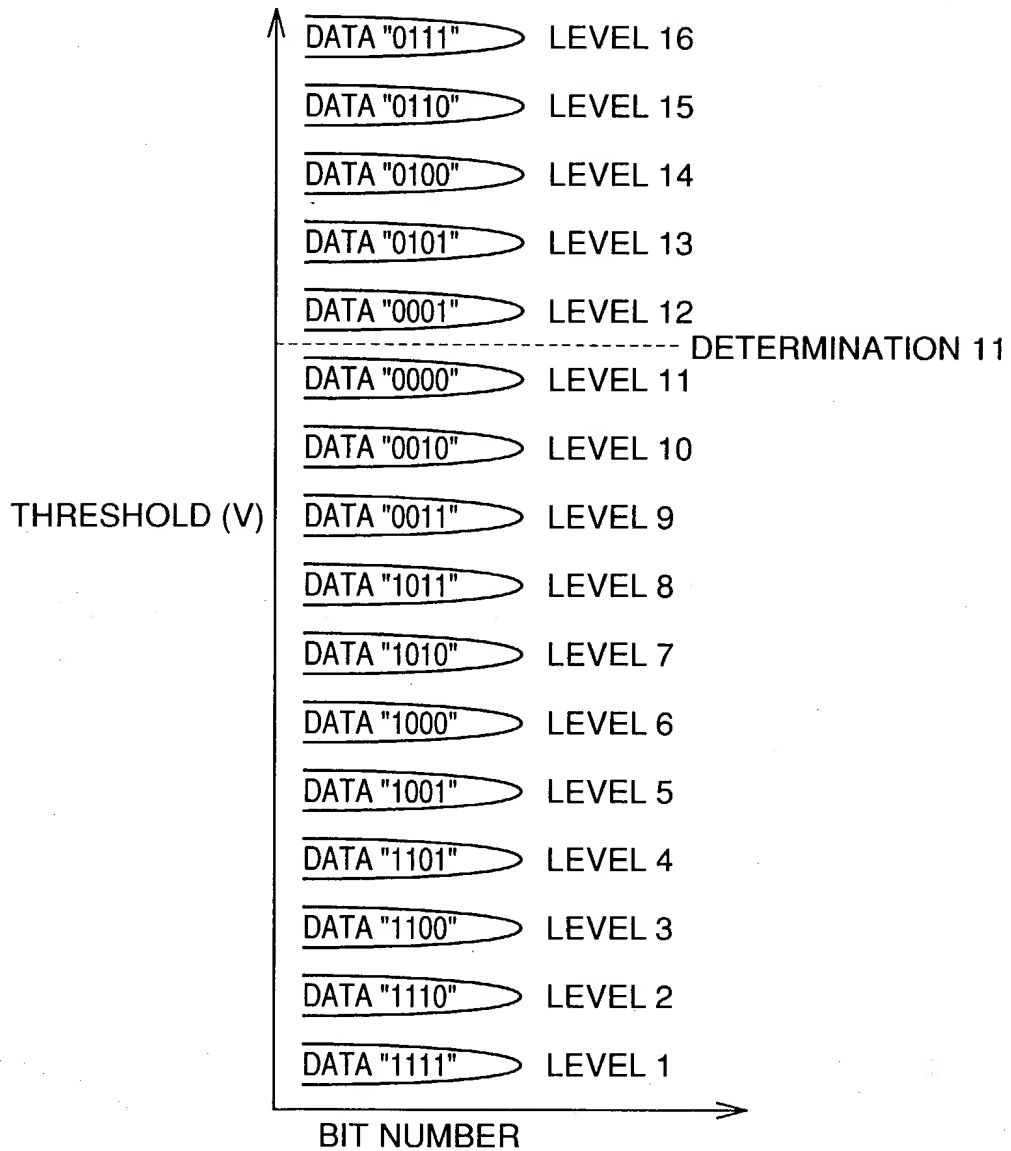




FIG.74

OR DATA OF DL-1 AND DL-4 TO DL-4			
DATA	I/O DATA	I/O DATA	I/O DATA
	0	0	0
	1	0	1
	2	0	2
	3	0	3
	4	0	4
	5	1	5
	6	1	6
	7	0	7
	0	0	0
	1	0	1
	2	0	2
	3	0	3
	4	0	4
	5	0	5
	6	0	6
	7	0	7
SL	DL-1	DL-2	DL-3
	OUTPUT (0Fh-F0h)		OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)



FIG.75

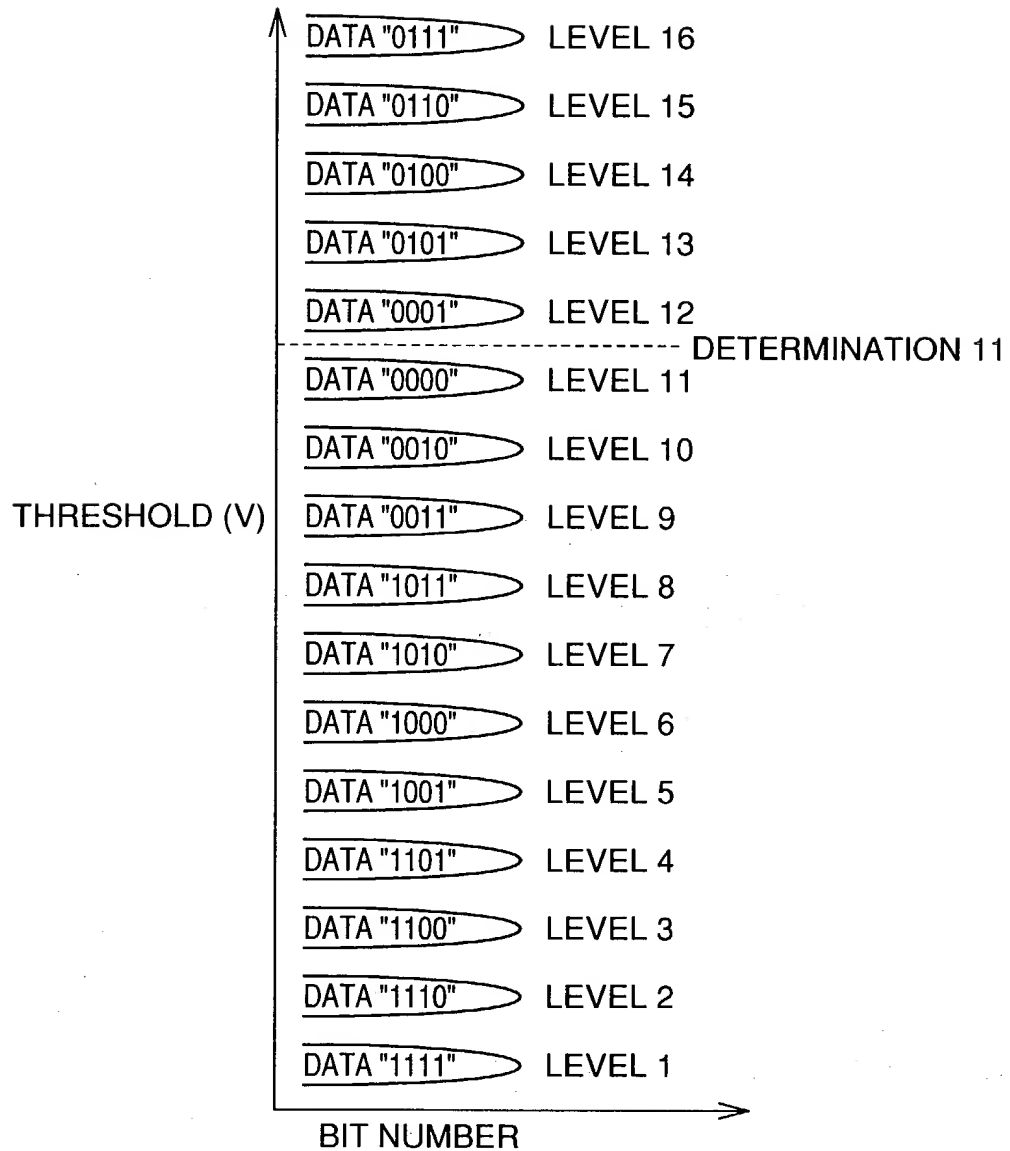


FIG.76

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0	→ TO DL-1	2	0	2	1
1		3	1	3	1
1		4	1	4	1
1		5	1	5	1
1		6	1	6	0
1		7	1	7	0
1		0	1	0	0
1		1	1	1	0
1		2	1	2	1
1		3	1	3	1
1		4	1	4	1
1		5	1	5	1
1		6	1	6	0
1		7	1	7	0
SL		DL-1	DL-2	DL-3	DL-4
			OUTPUT (00h-FFh)	OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)	



FIG.77

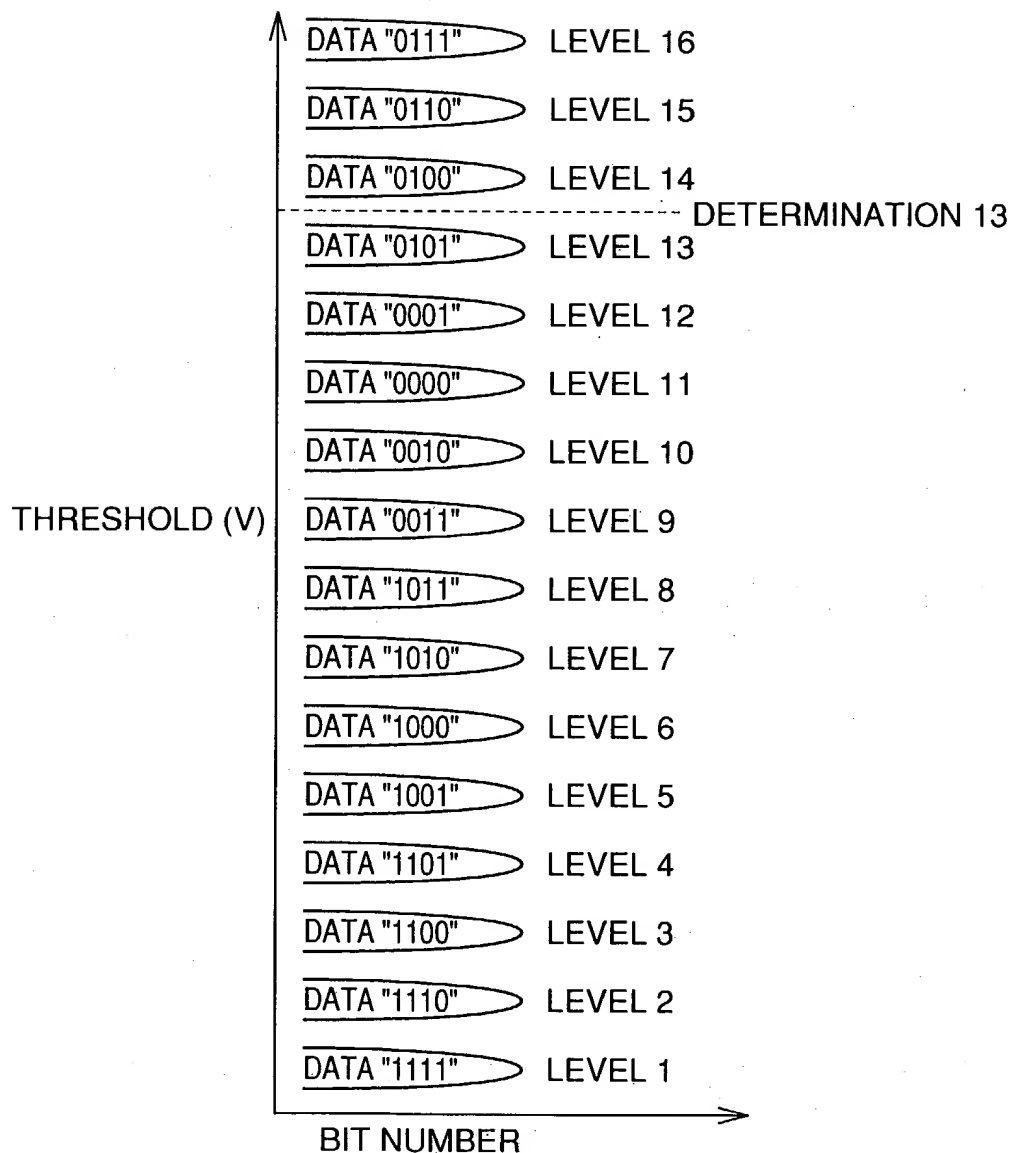




FIG.78

		OR DATA OF DL-1 AND DL-4 TO DL-4							
DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0	0	0	0	0
1		1	1	1	0	1	0	1	0
1	NOR INVERTED DATA OF SL AND DATA OF DL-1 TO DL-1	2	1	2	0	2	1	2	0
1		3	0	3	0	3	1	3	0
1		4	0	4	1	4	1	4	0
1		5	0	5	1	5	1	5	1
1		6	0	6	1	6	0	6	1
1		7	0	7	1	7	0	7	0
1		0	0	0	1	0	0	0	0
1		1	0	1	1	1	0	1	1
1		2	0	2	1	2	1	2	1
1		3	0	3	1	3	1	3	0
1		4	0	4	0	4	1	4	0
1		5	0	5	0	5	1	5	1
1		6	0	6	0	6	0	6	1
1		7	0	7	0	7	0	7	0
SL		DL-1	DL-2	DL-3	DL-4				
		OUTPUT (0Fh-F0h)		OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)					



FIG.79

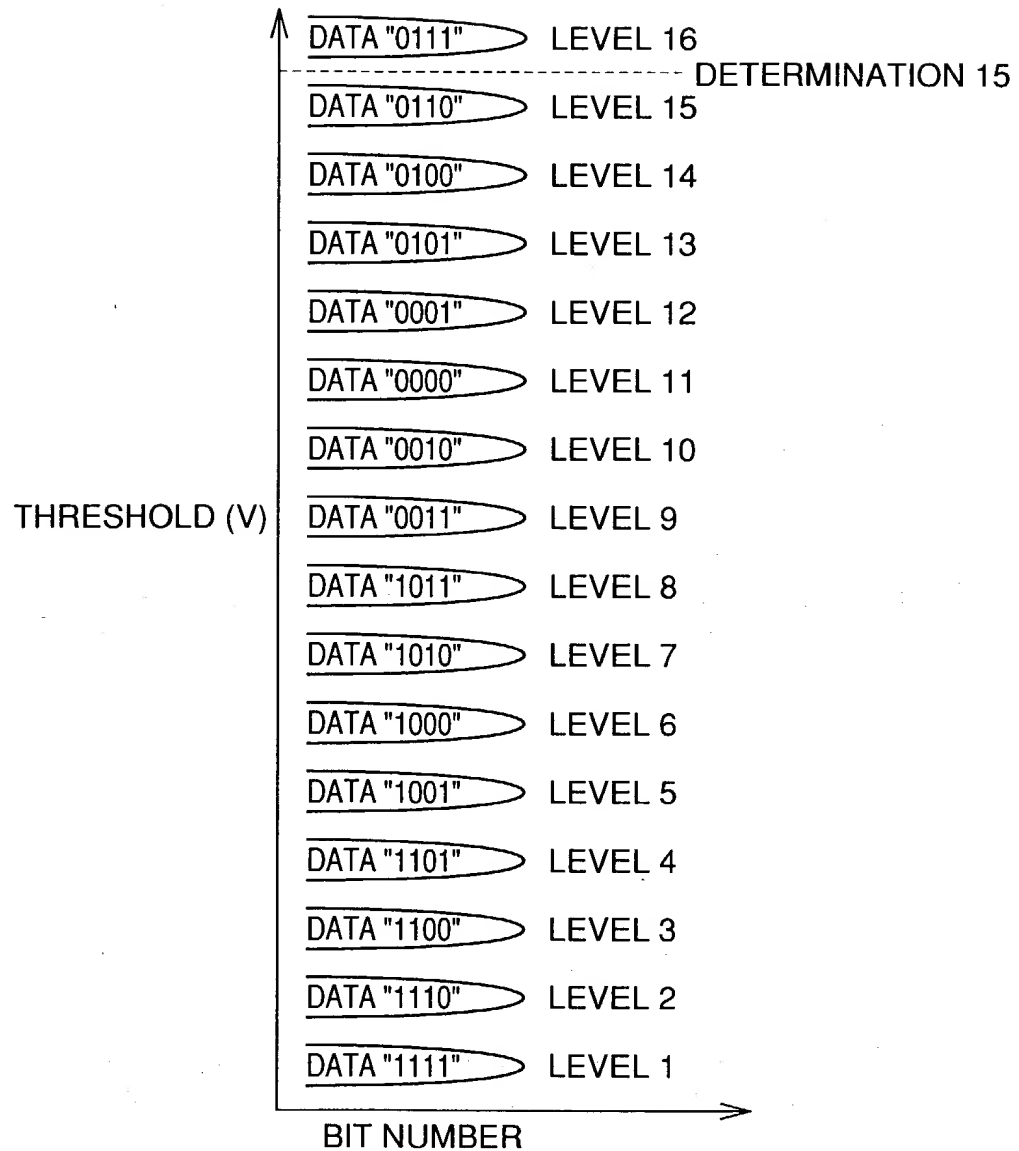


FIG.80

OR DATA OF DL-1 AND DL-4 TO DL-4								
DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA			
		0	0	0	0	0	0	0
		1	1	1	0	1	0	1
		2	1	2	0	2	1	1
		3	0	3	0	3	1	0
		4	0	4	1	4	1	0
		5	0	5	1	5	1	1
		6	0	6	1	6	0	1
		7	0	7	1	7	0	0
		0	0	0	1	0	0	0
		1	0	1	1	1	0	1
		2	0	2	1	2	1	1
		3	0	3	1	3	1	0
		4	0	4	0	4	1	0
		5	0	5	0	5	1	1
		6	0	6	0	6	0	1
		7	0	7	0	7	0	0
SL		DL-1	DL-2	DL-3	DL-4			
		OUTPUT (0Fh-F0h)		OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)				



FIG.81

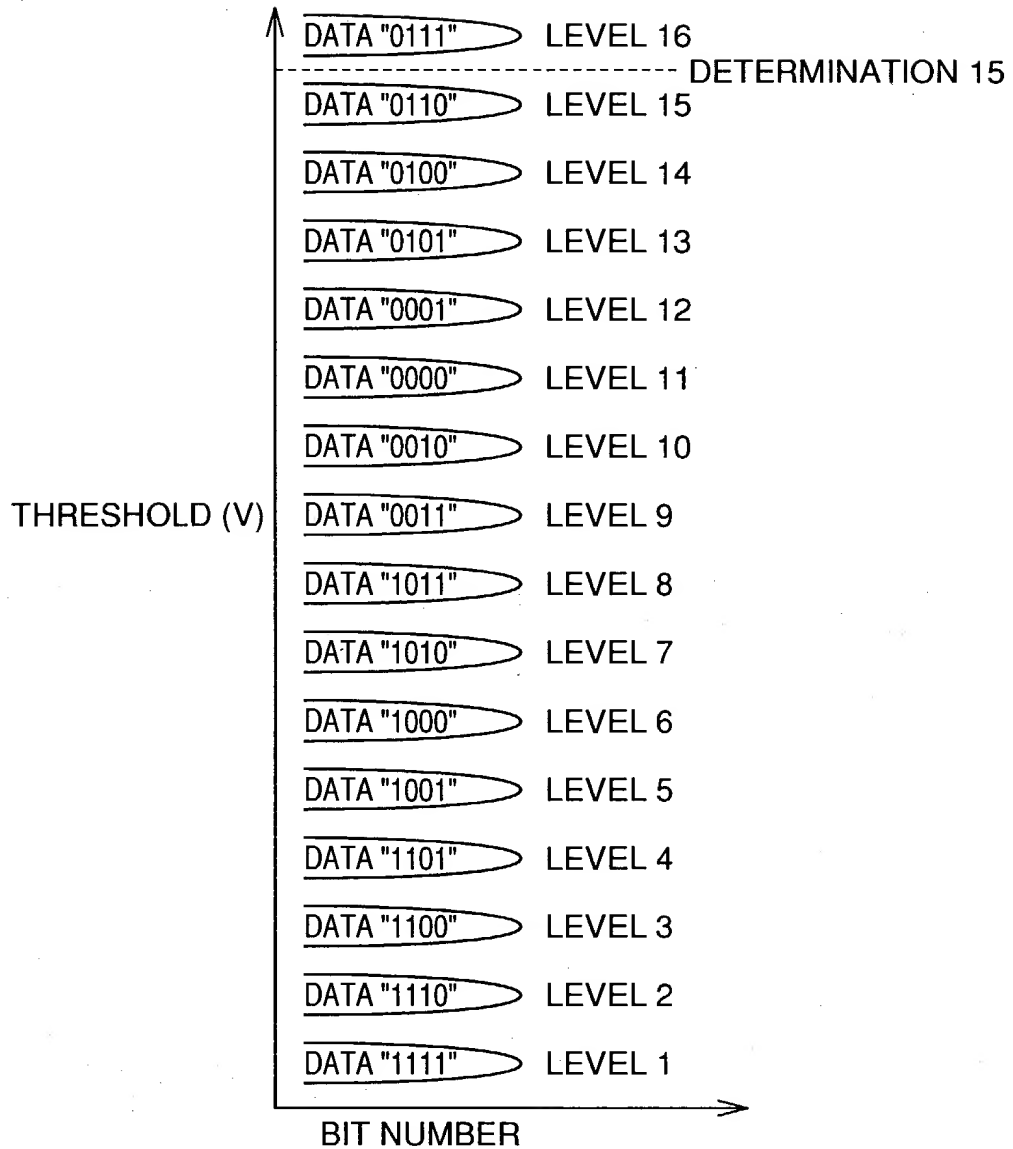
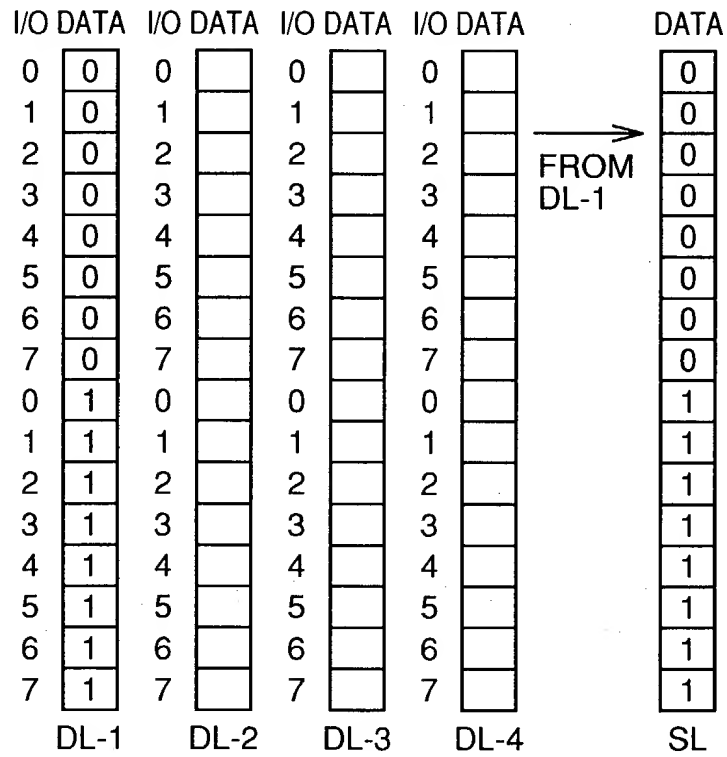




FIG.82



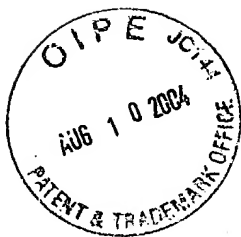


FIG.83

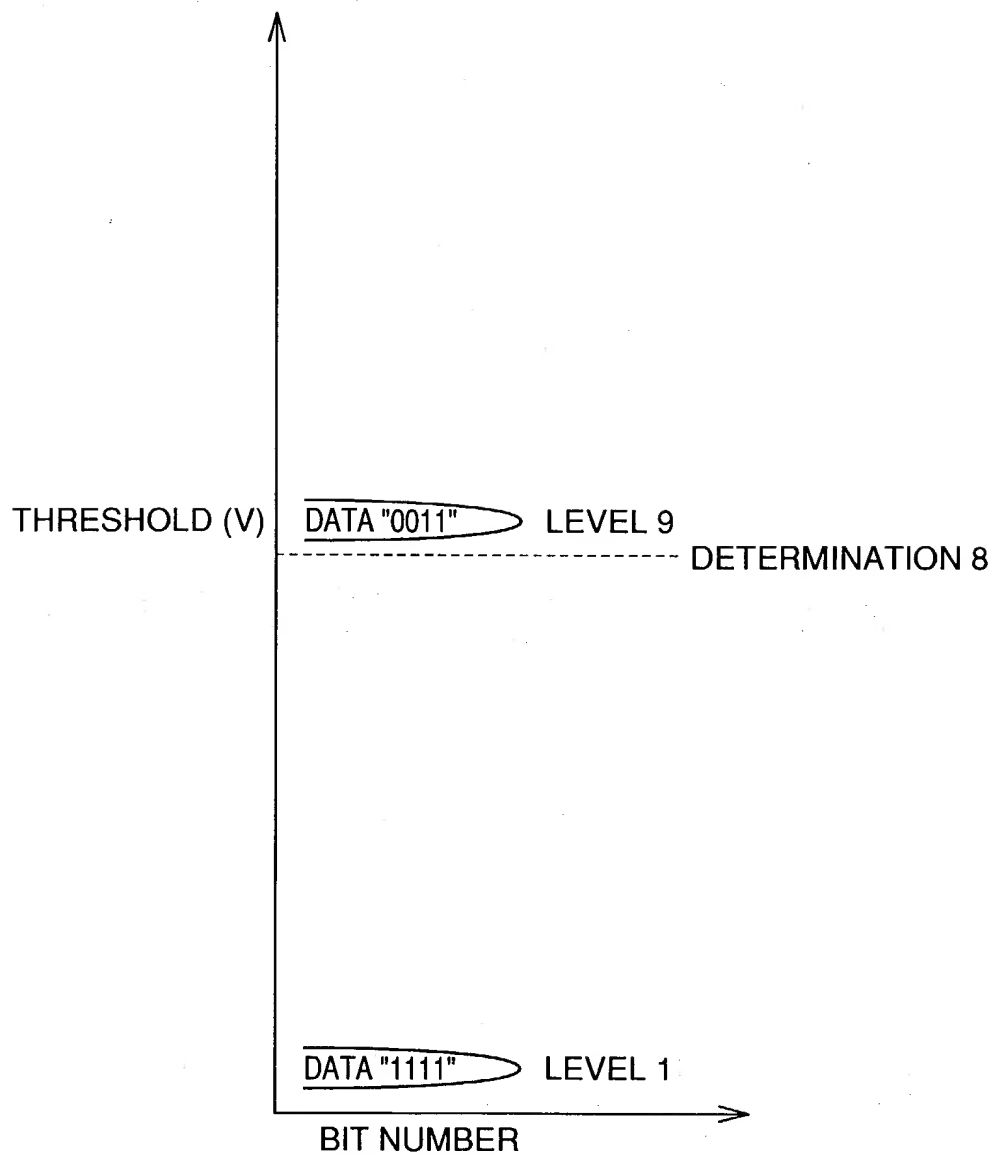




FIG.84

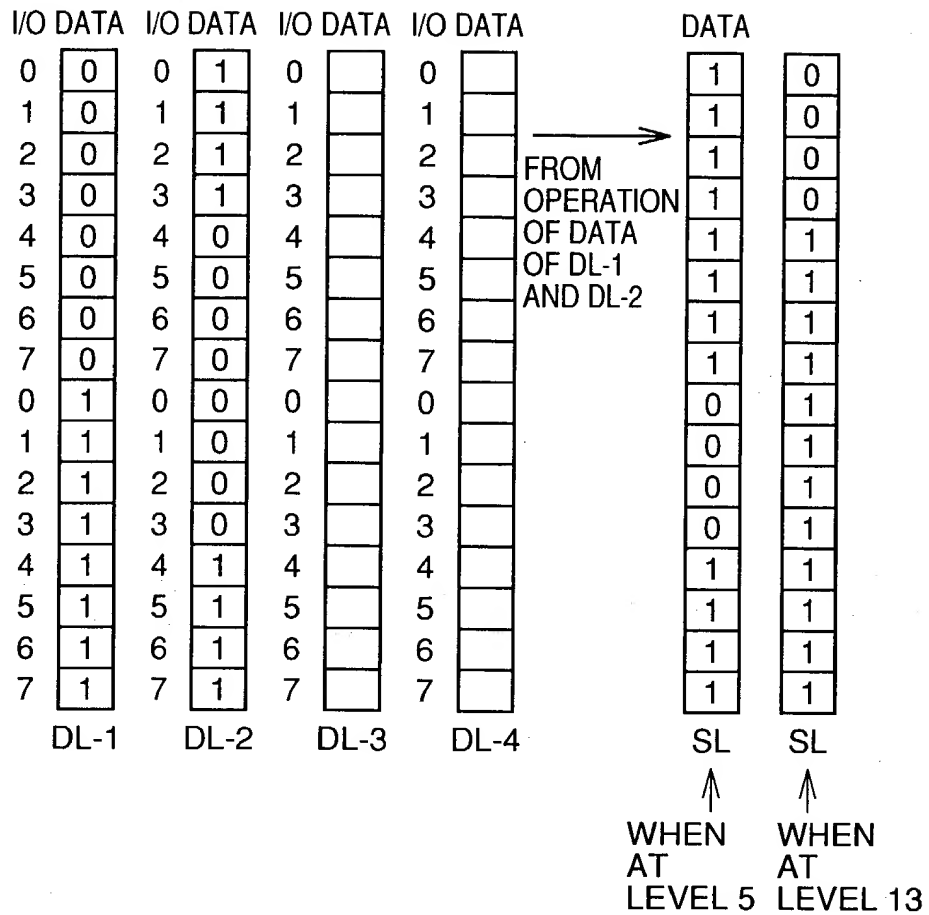




FIG.85

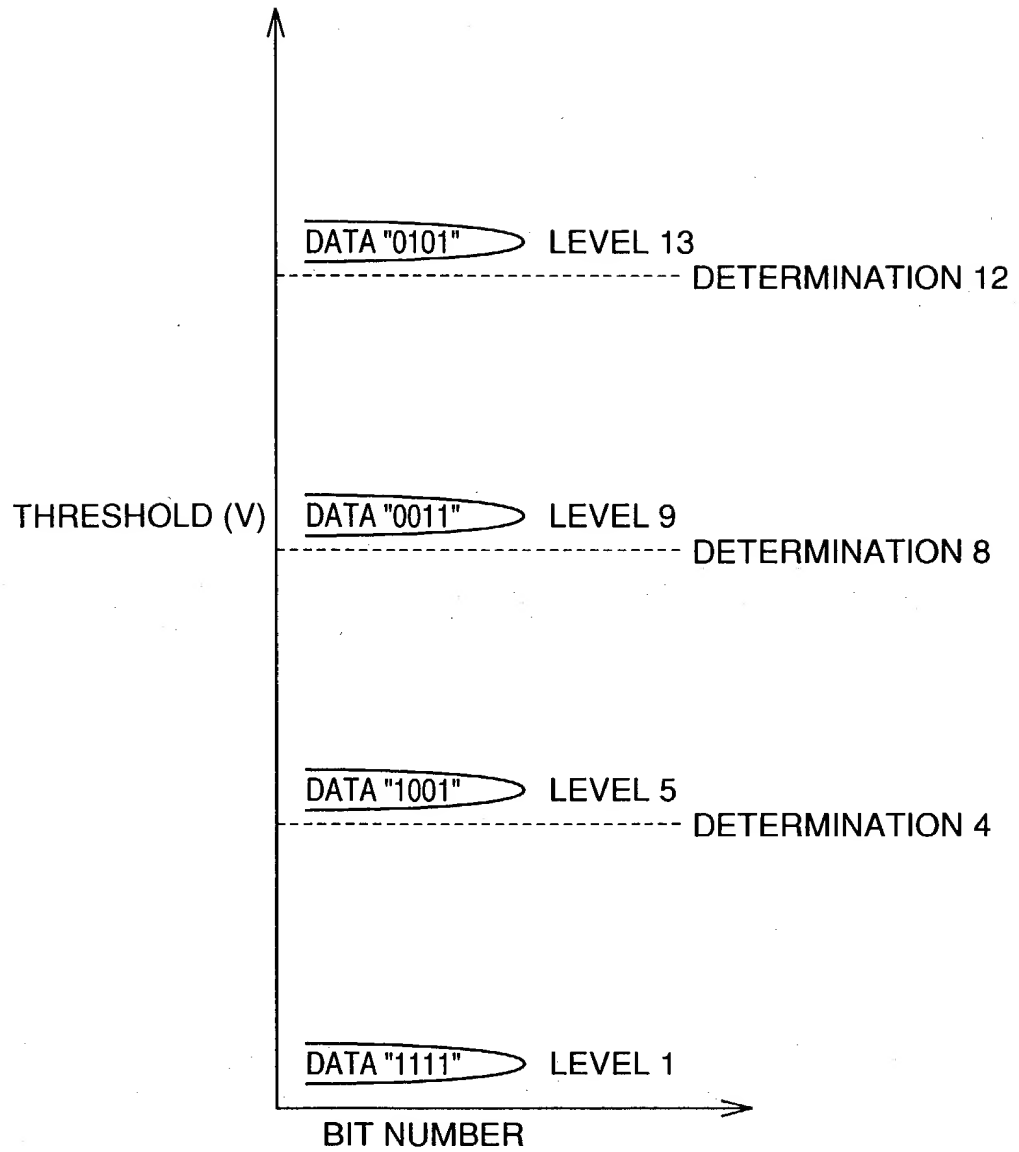


FIG.86

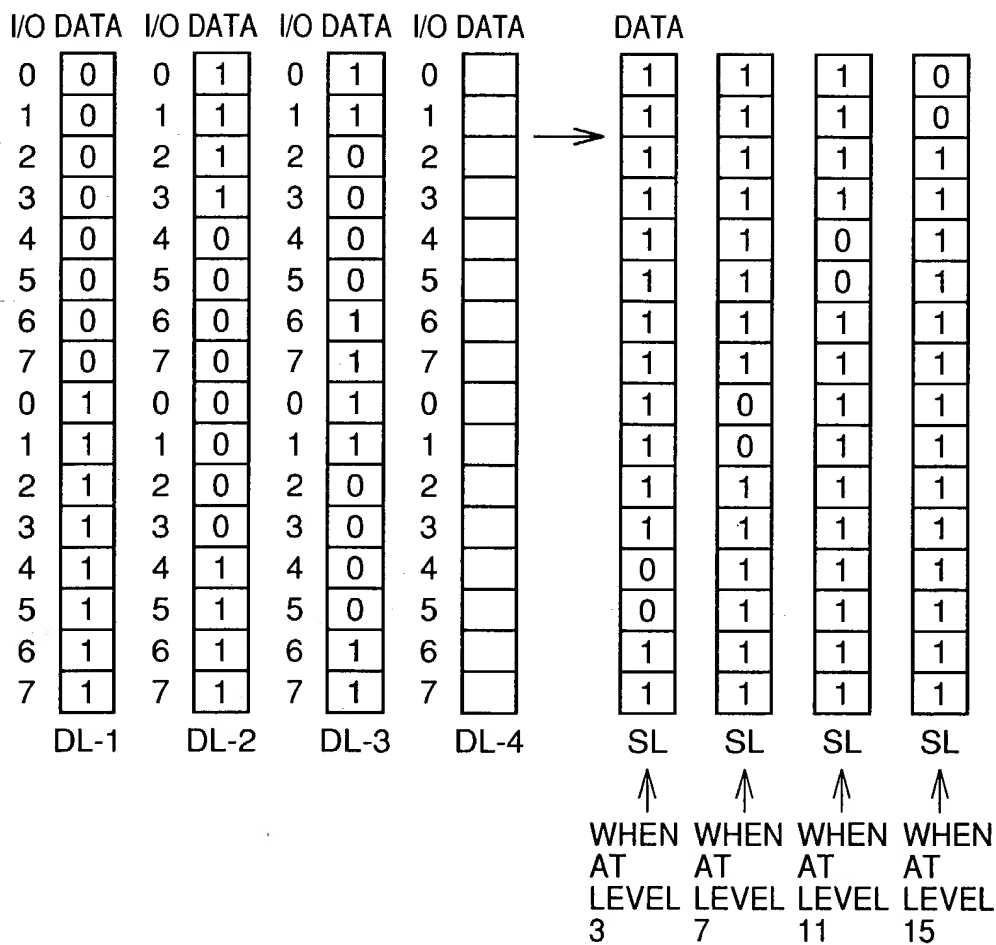




FIG.87

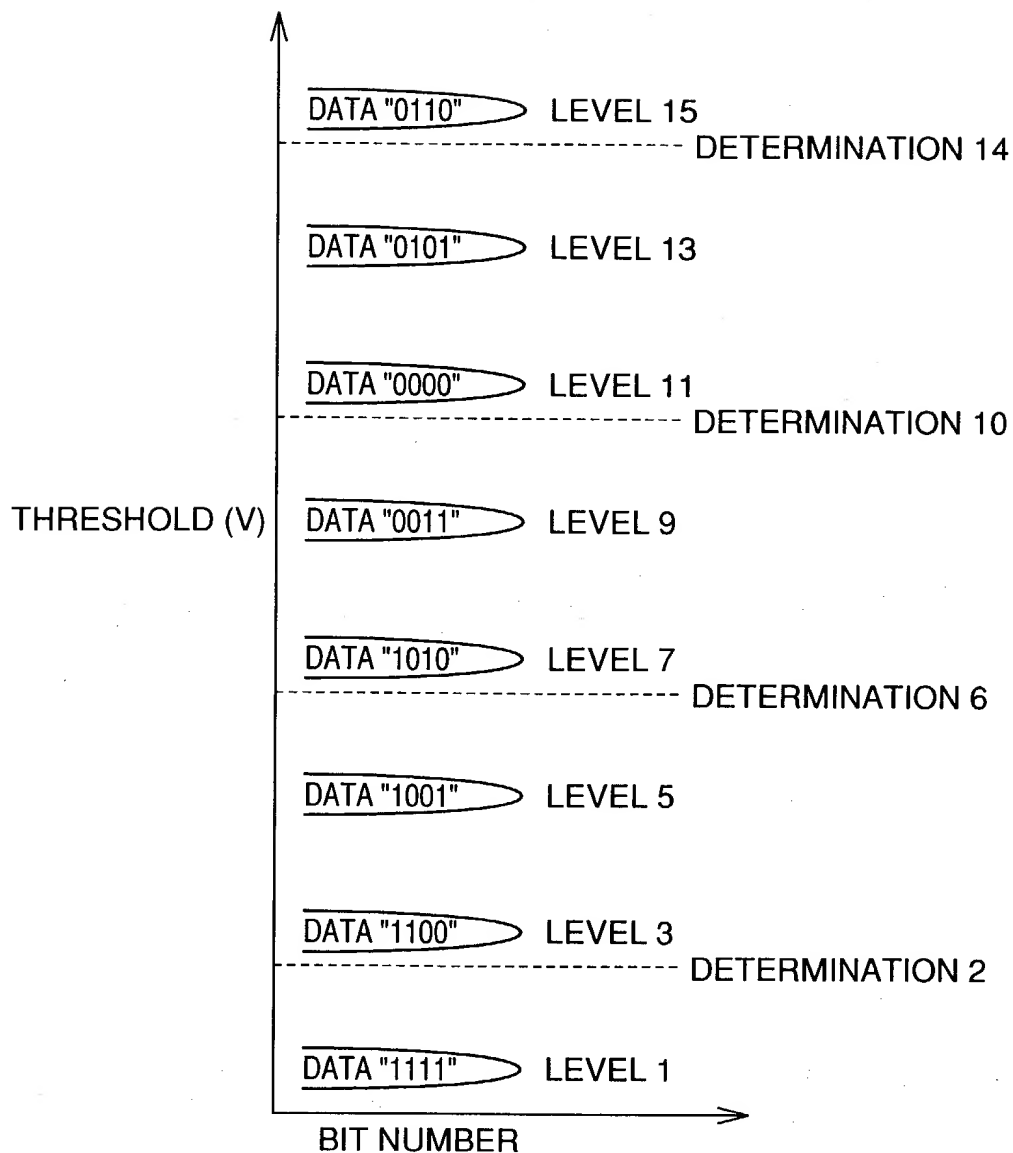




FIG.89

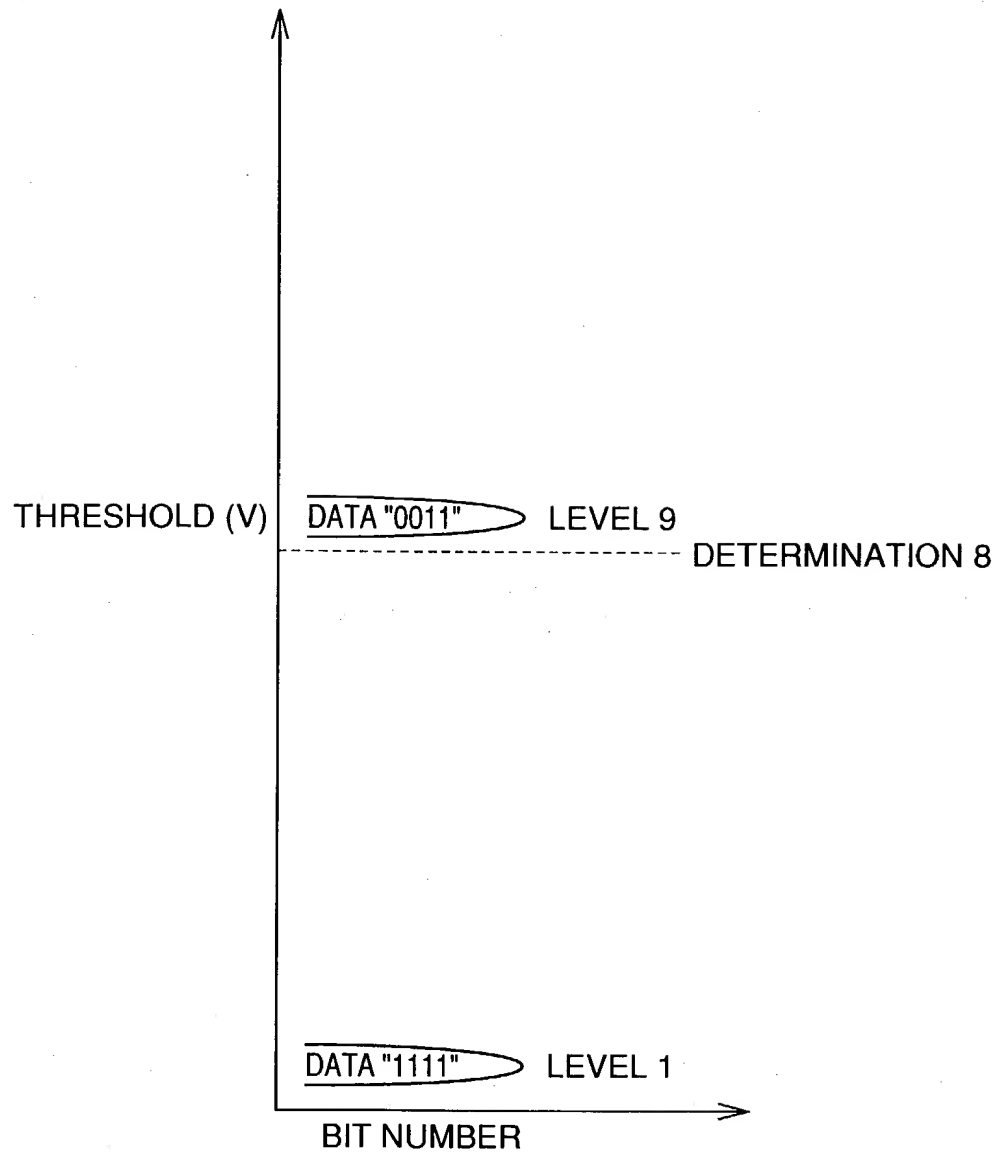




FIG.90

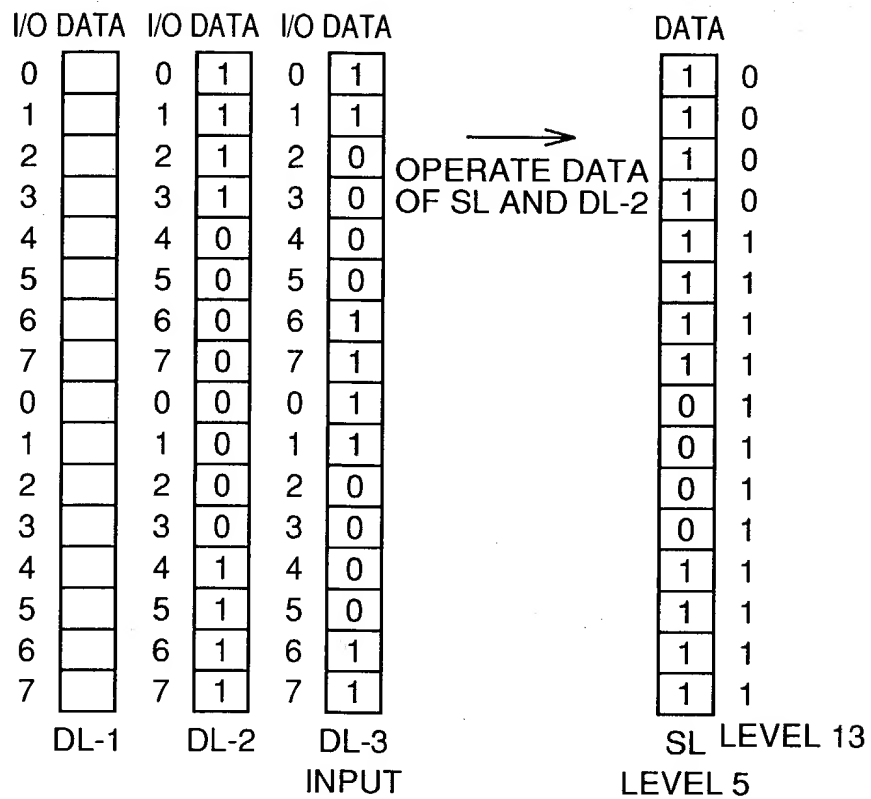


FIG.91

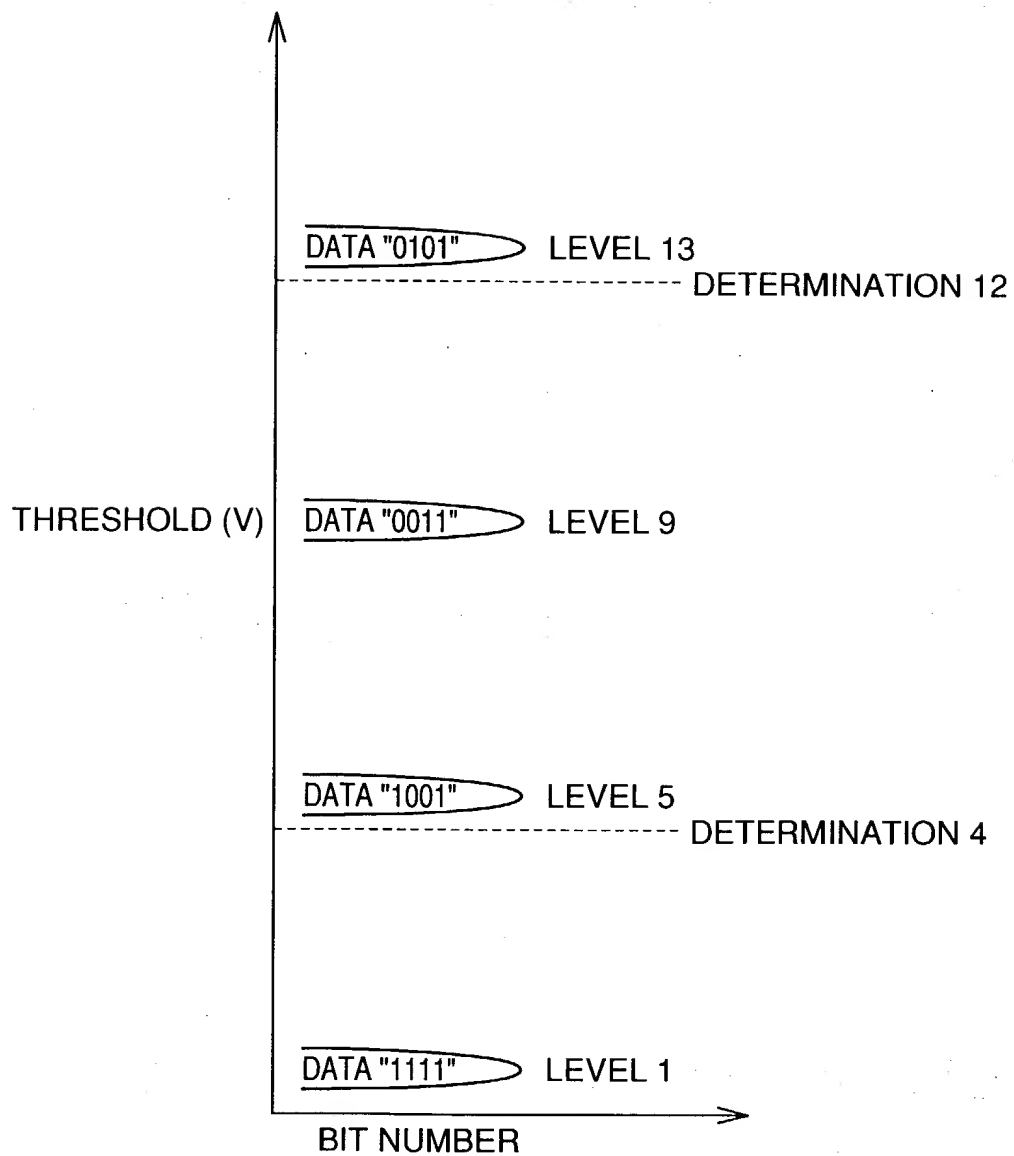
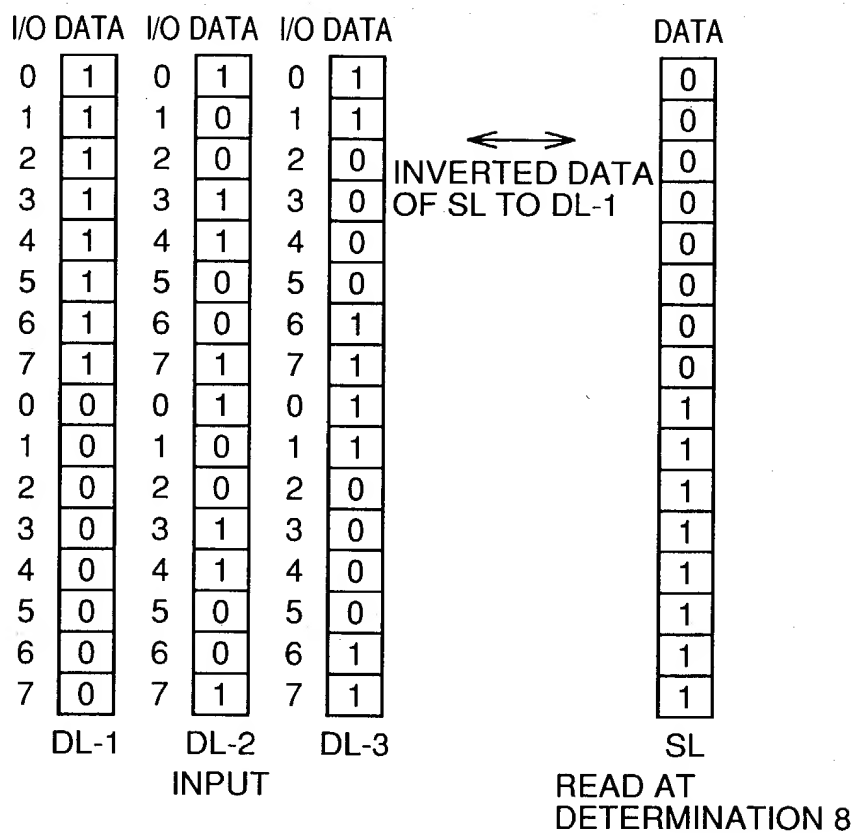


FIG.92



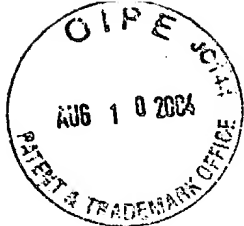


FIG.93

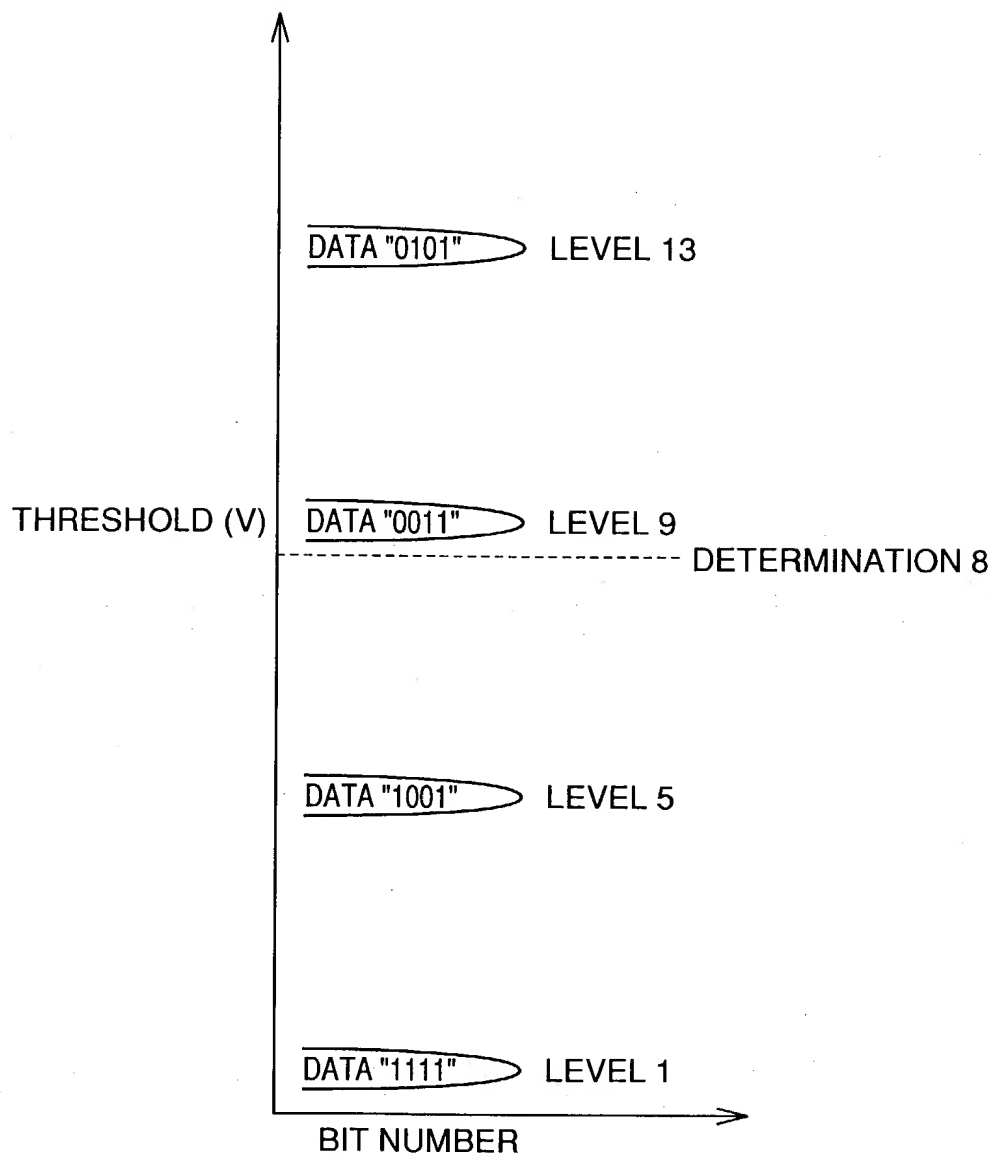
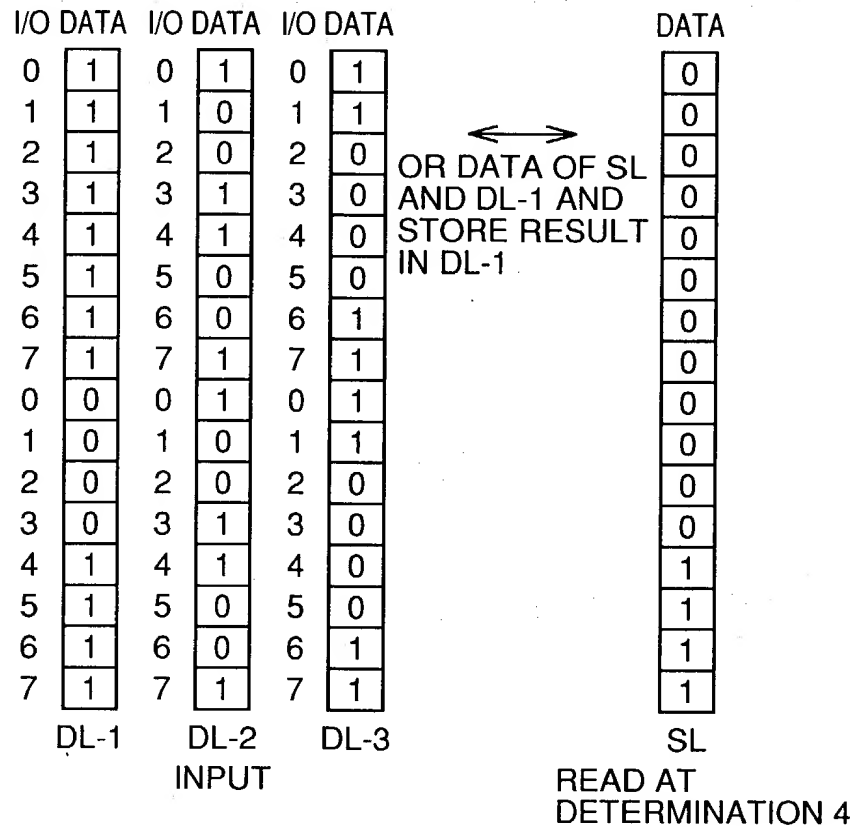


FIG.94



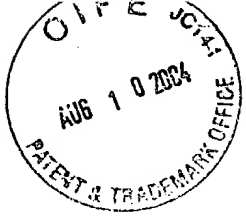


FIG.95

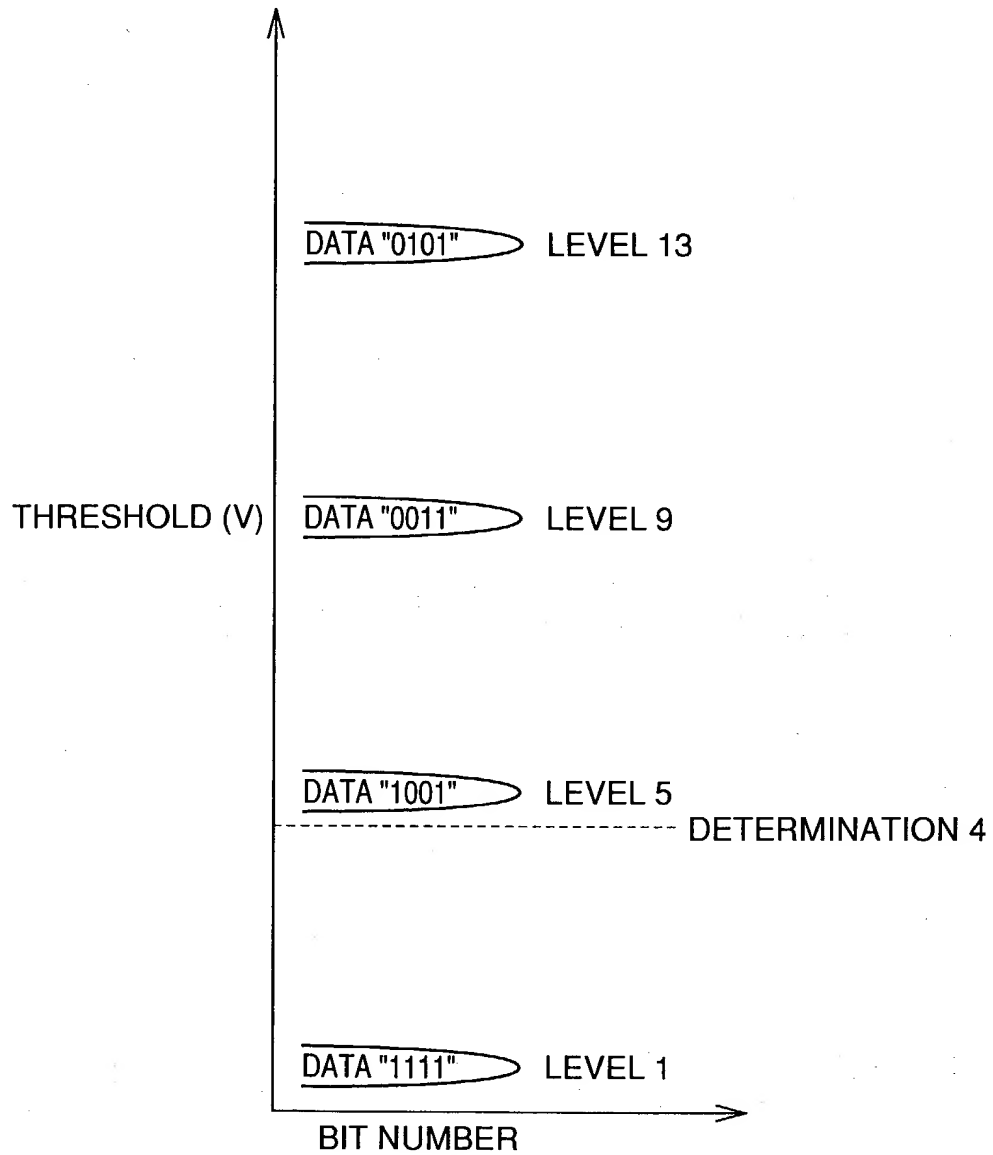
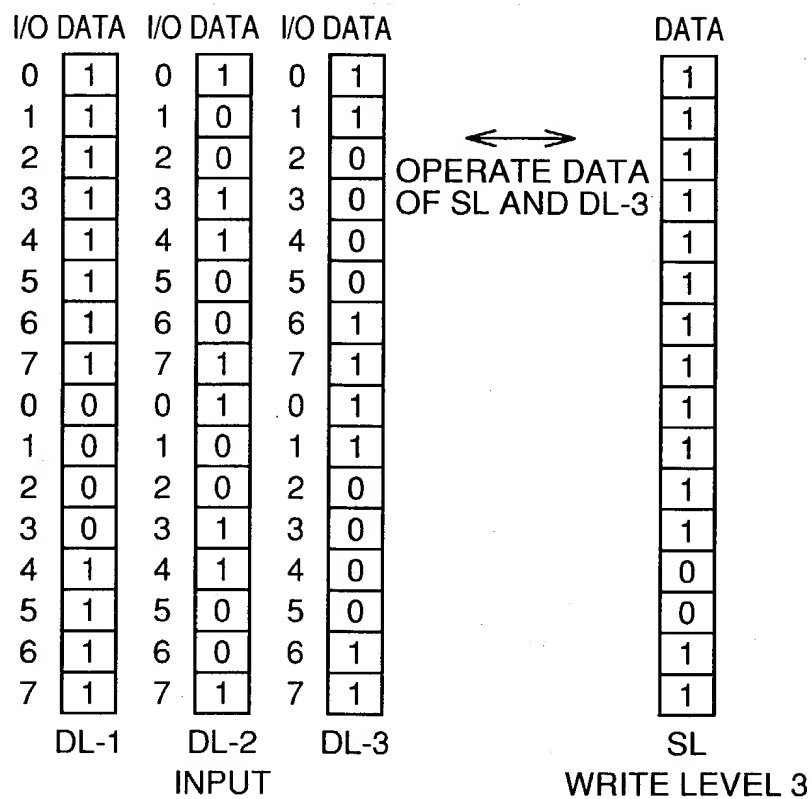


FIG.96



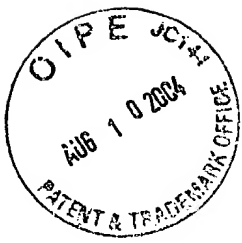


FIG.97

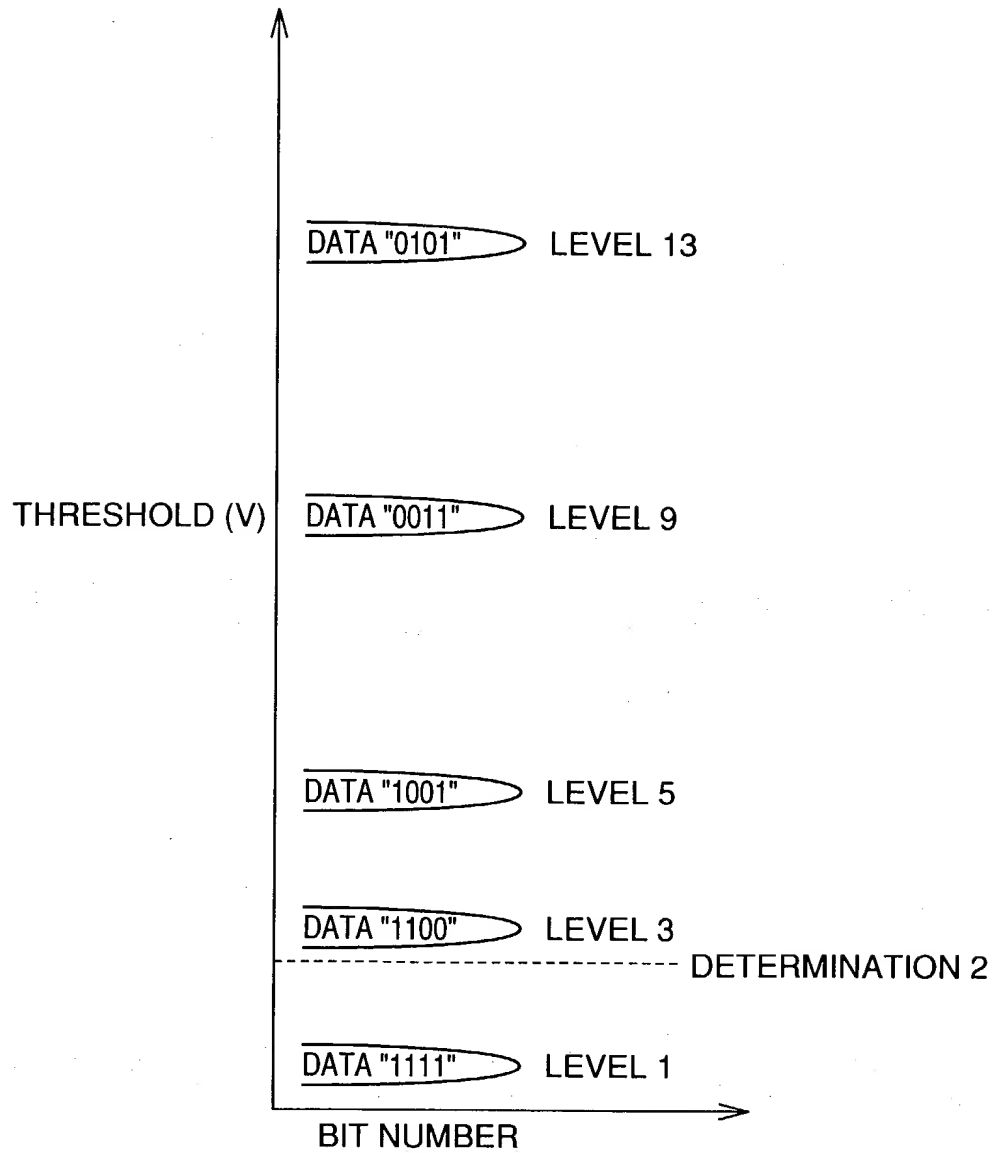




FIG.98

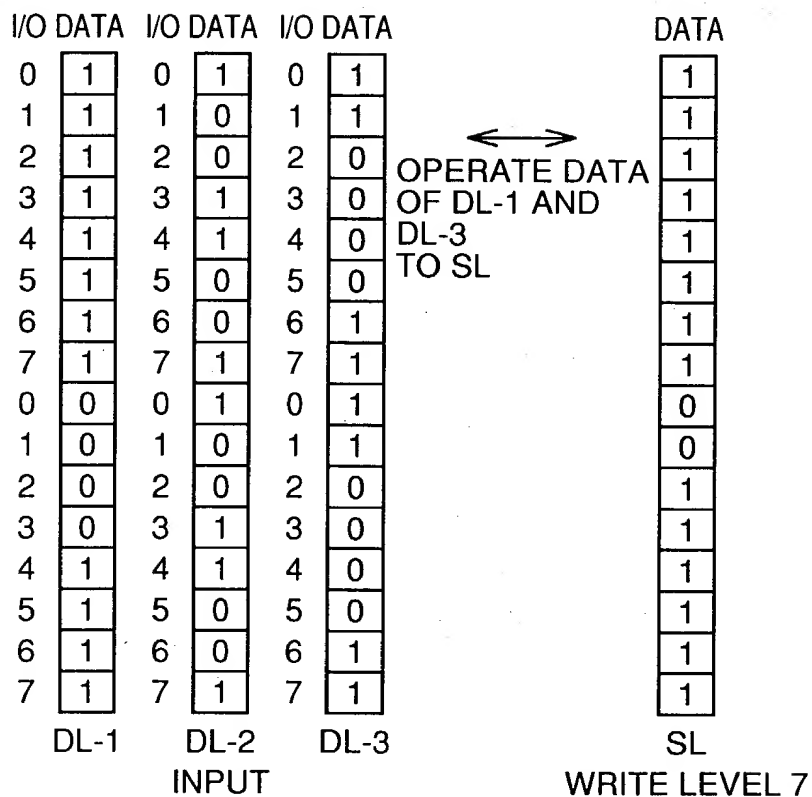




FIG.99

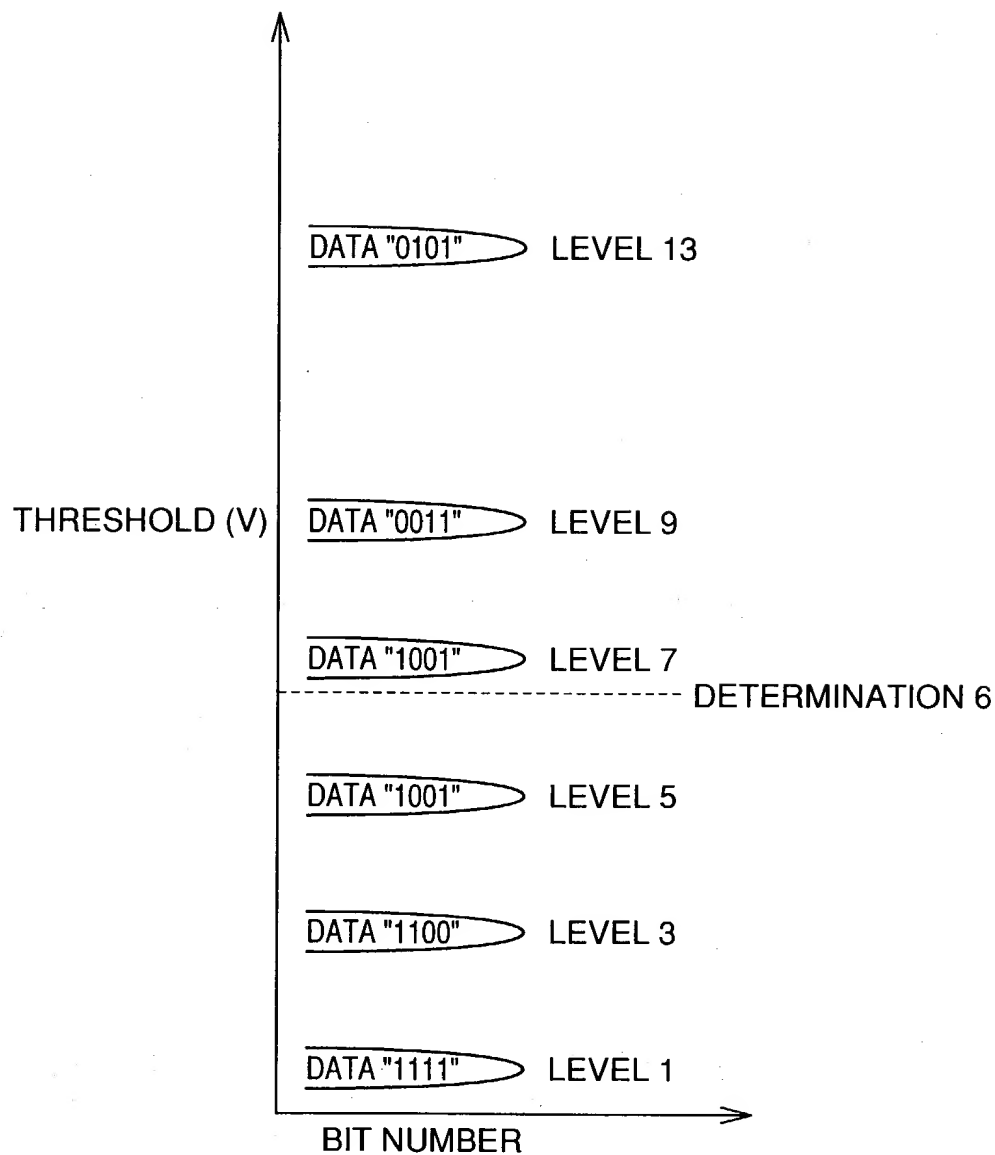
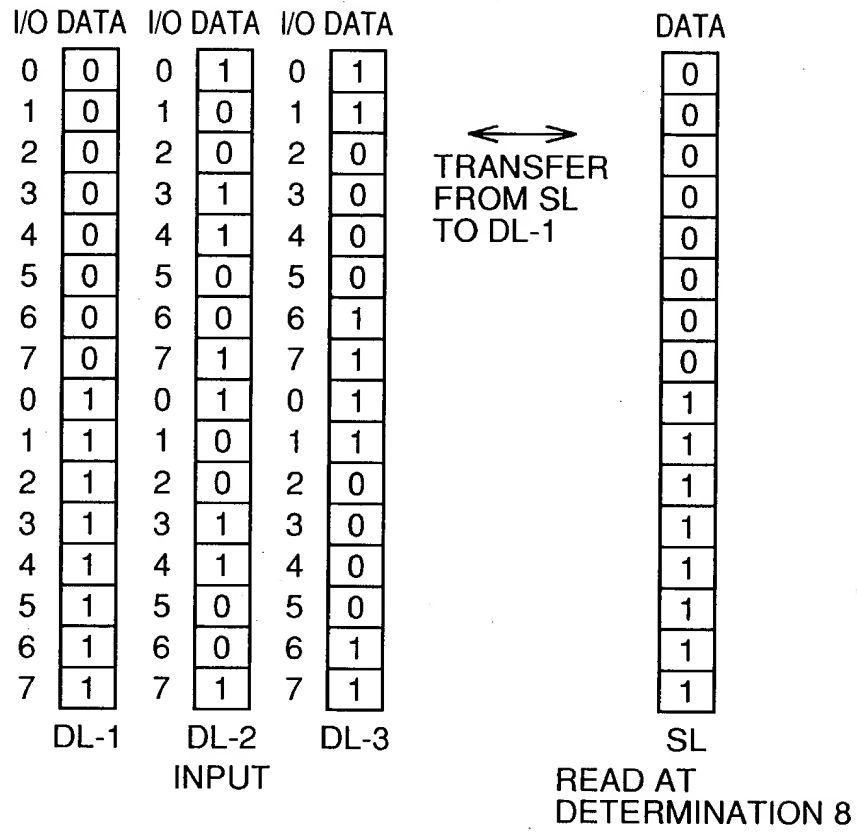


FIG. 100



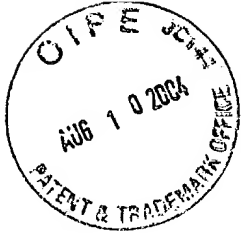


FIG.101

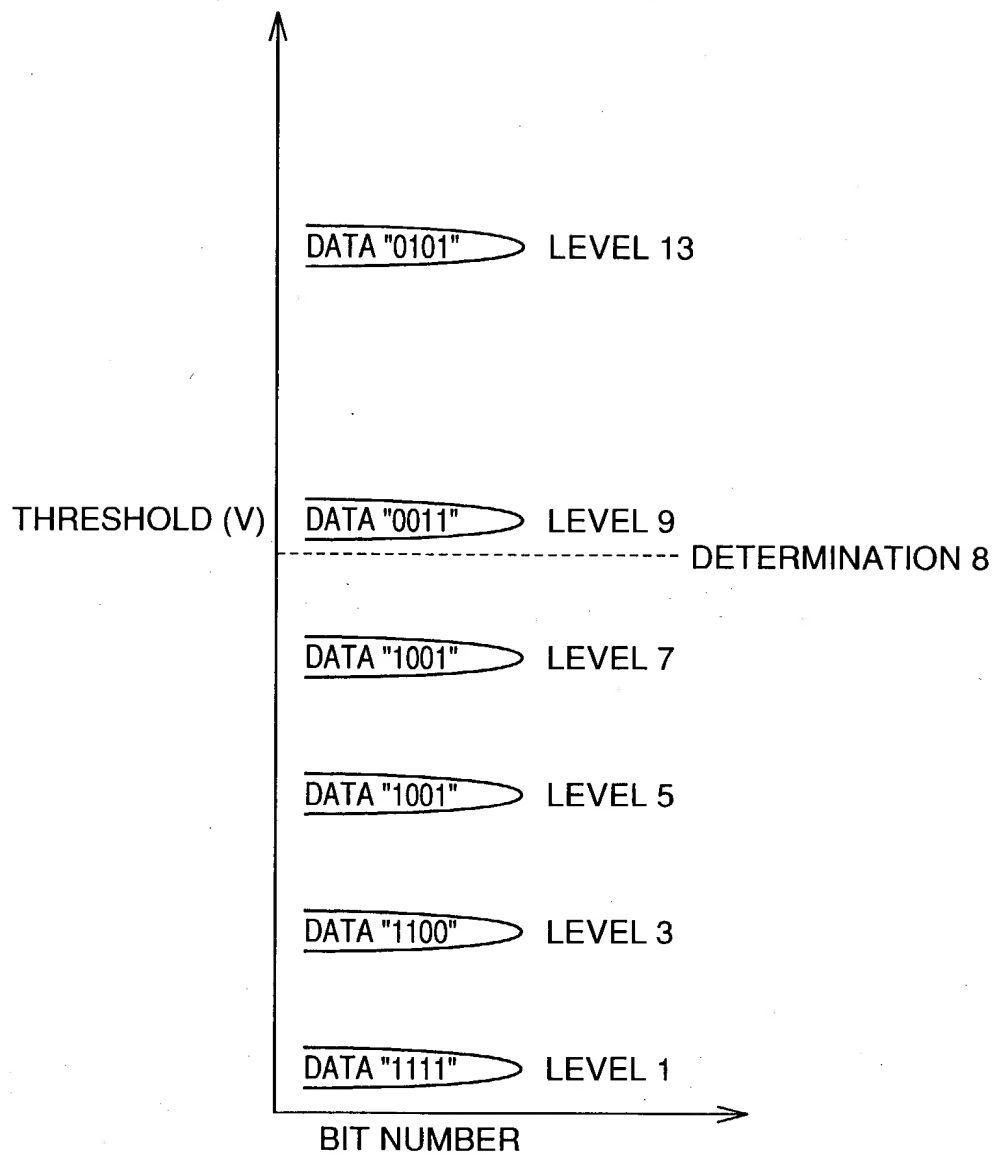


FIG. 102

I/O DATA	I/O DATA	I/O DATA		DATA
0 1	0 1	0 1		0
1 1	1 0	1 1		0
2 1	2 0	2 0	↔	0
3 1	3 1	3 0	OR INVERTED	0
4 0	4 1	4 0	DATA OF SL	1
5 0	5 0	5 0	AND DATA OF	1
6 0	6 0	6 1	DL-1 AND	1
7 0	7 1	7 1	STORE RESULT	1
			IN DL-1	1
0 1	0 1	0 1		1
1 1	1 0	1 1		1
2 1	2 0	2 0		1
3 1	3 1	3 0		1
4 1	4 1	4 0		1
5 1	5 0	5 0		1
6 1	6 0	6 1		1
7 1	7 1	7 1		1
DL-1	DL-2	DL-3		SL
	INPUT			READ AT
				DETERMINATION 12

FIG. 103

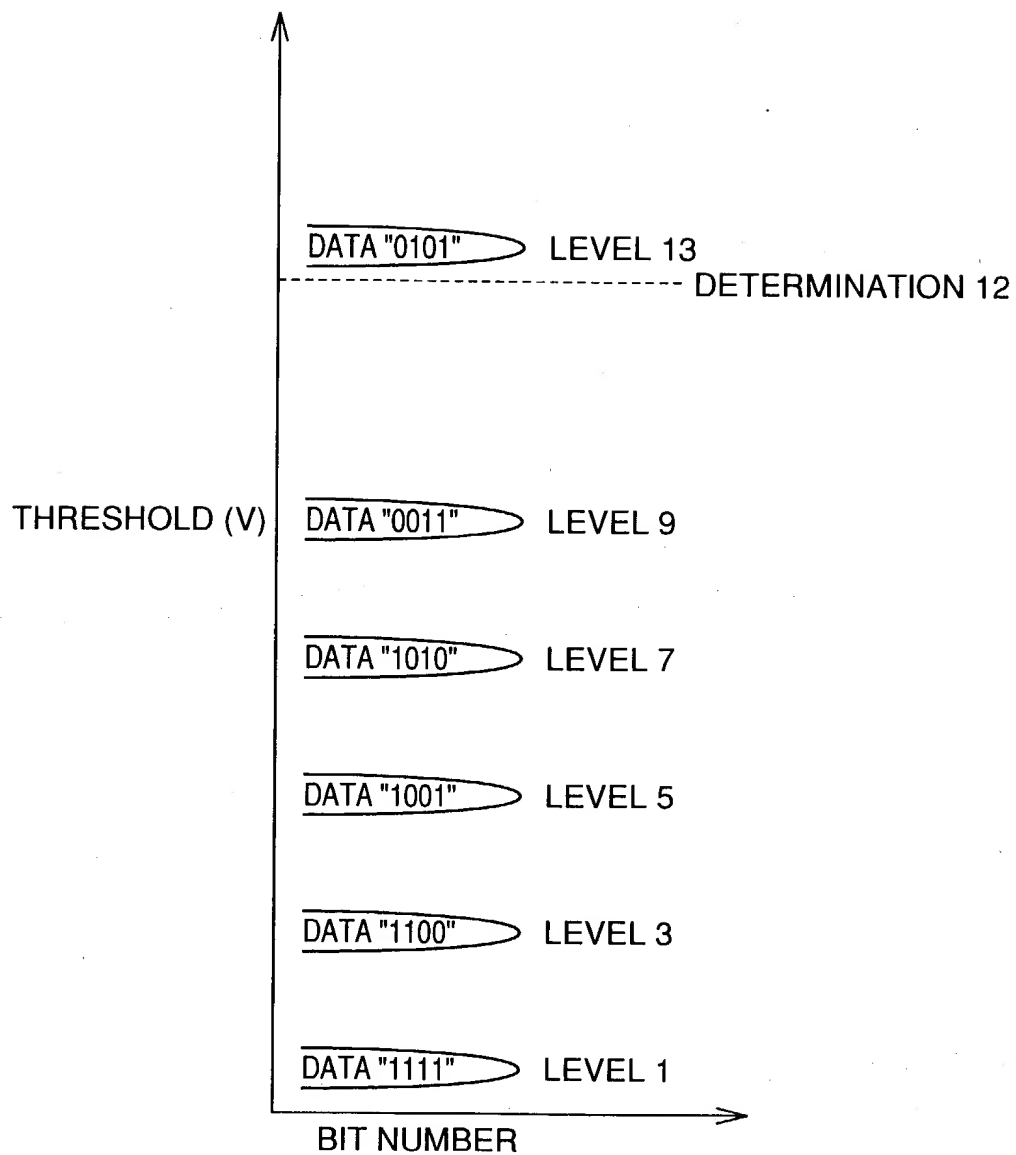
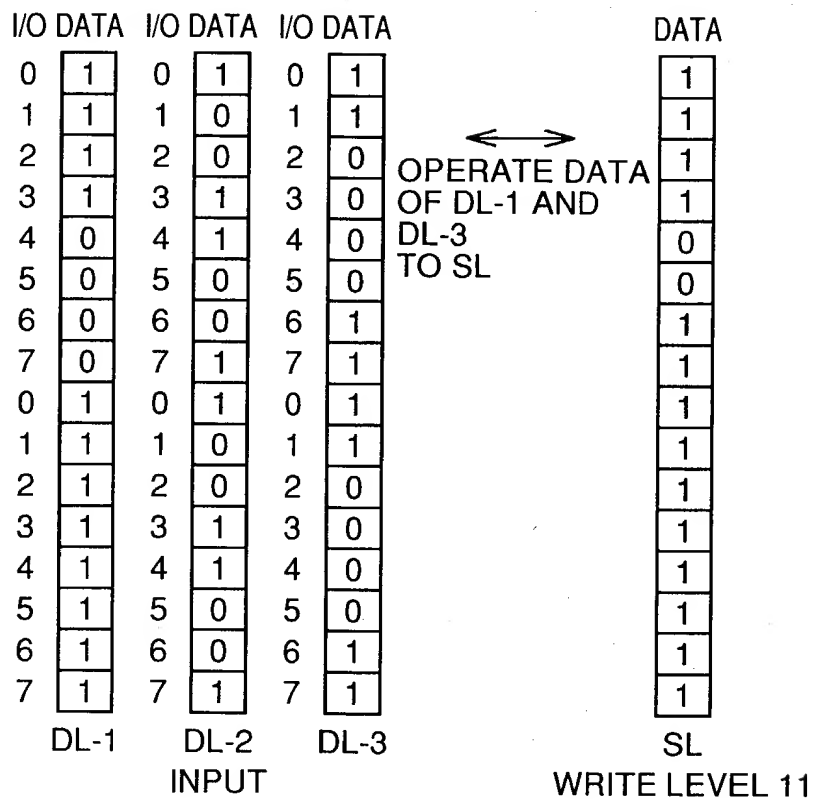


FIG. 104



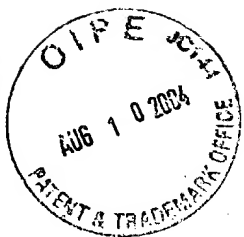


FIG. 105

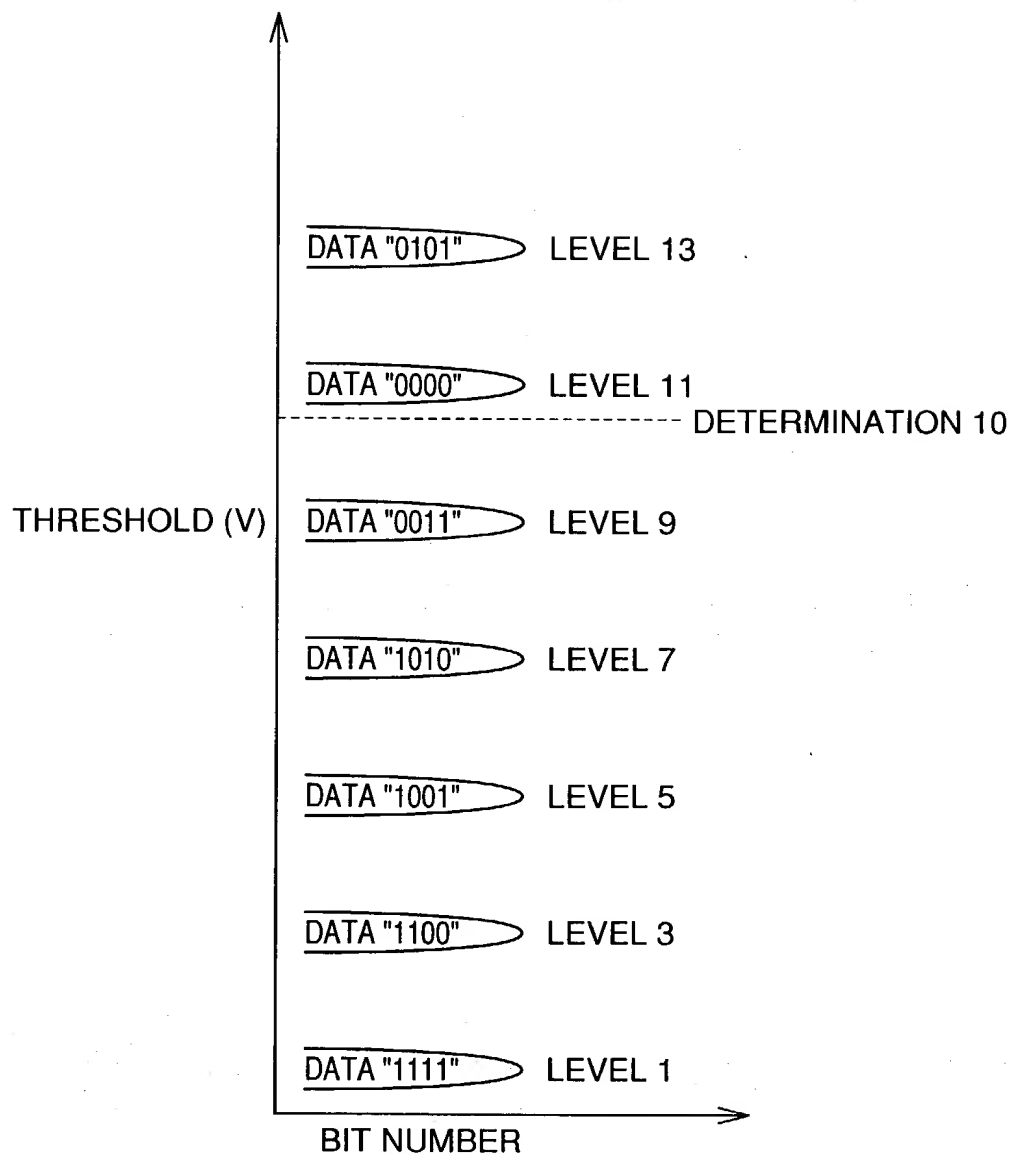


FIG. 106

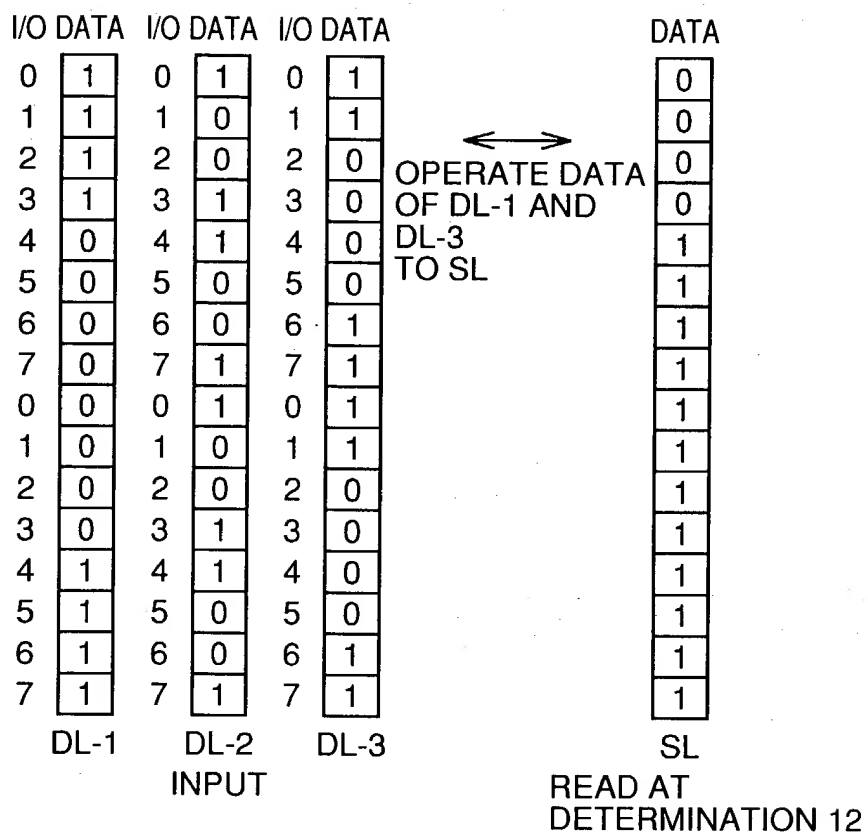




FIG. 107

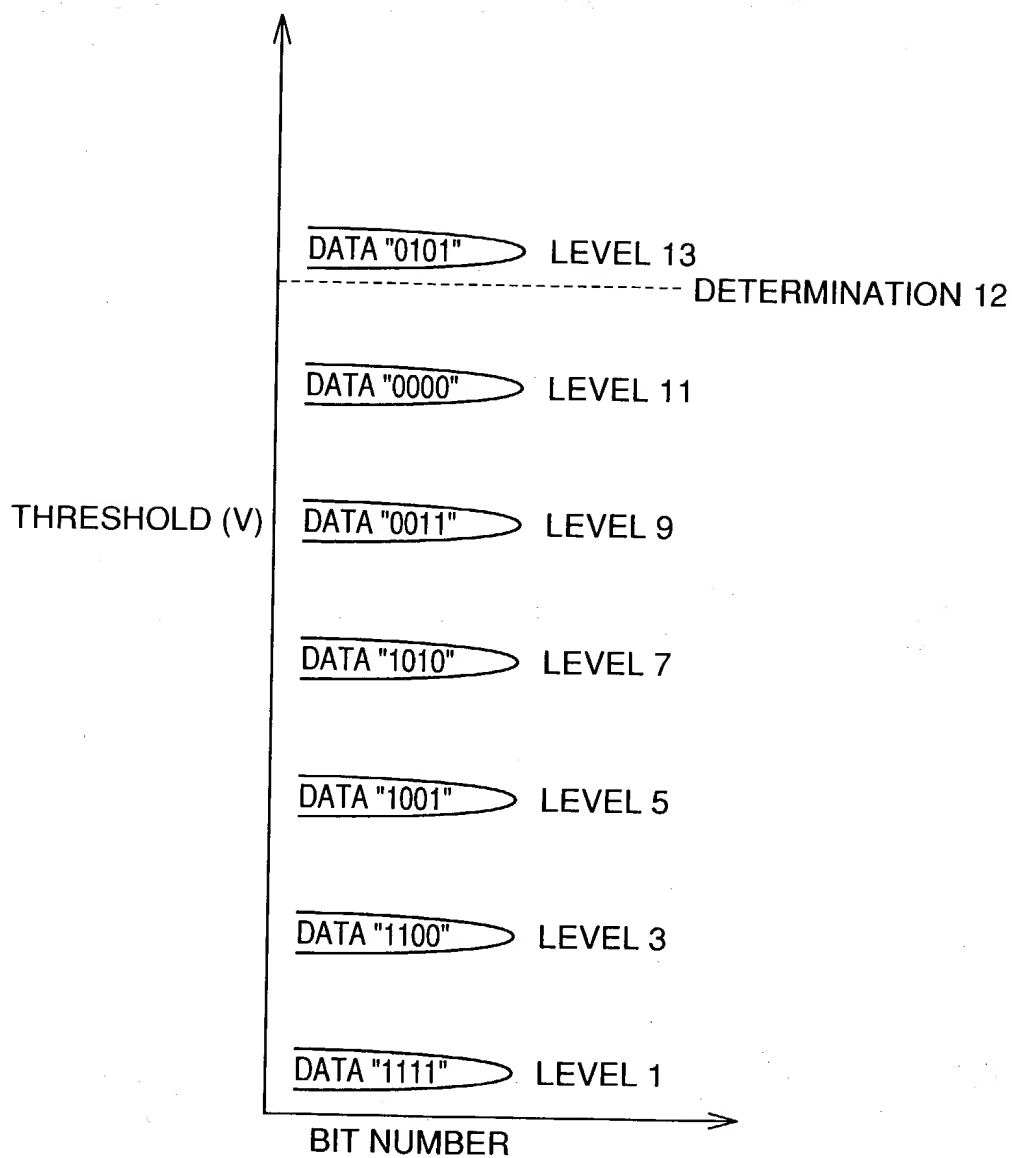


FIG.108

I/O DATA	I/O DATA	I/O DATA
0	0	0
1	1	1
2	0	0
3	1	0
4	1	0
5	0	0
6	0	1
7	1	1
0	0	1
1	1	1
2	0	0
3	1	0
4	1	0
5	0	0
6	0	1
7	1	1
DL-1	DL-2	DL-3
INPUT		

DATA
0
0
1
1
1
1
1
1
1
1
1
1
1
1
1
1
SL
WRITE LEVEL 15



FIG. 109

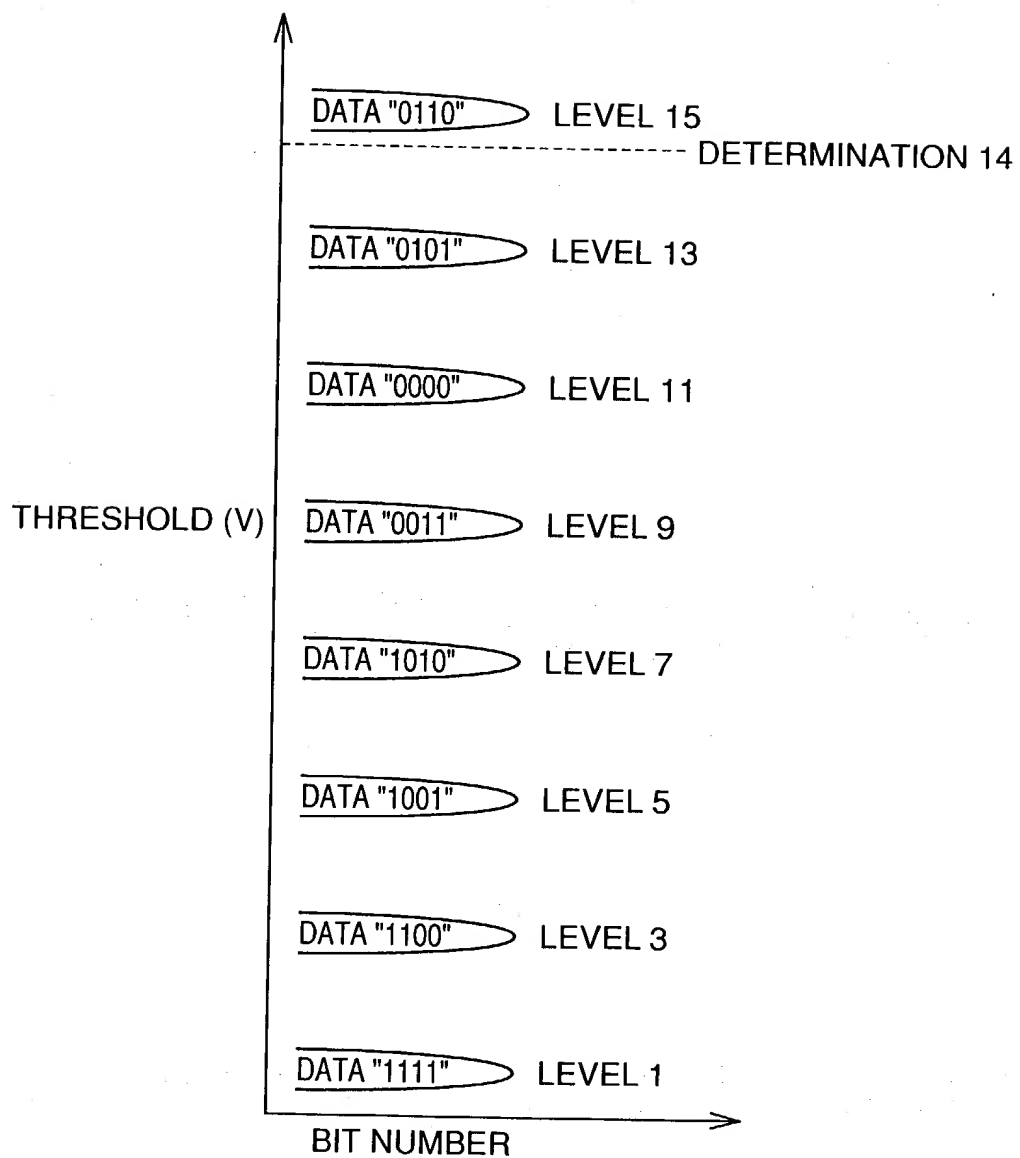




FIG. 110

I/O DATA		I/O DATA		I/O DATA		DATA	
0	0	0	1	0		0	
1	0	1	0	1		0	
2	0	2	0	2		0	
3	0	3	1	3		0	
4	0	4	1	4		0	
5	0	5	0	5		0	
6	0	6	0	6		0	
7	0	7	1	7		0	
0	0	0	1	0		0	
1	0	1	0	1		0	
2	0	2	0	2		0	
3	0	3	1	3		0	
4	0	4	1	4		0	
5	0	5	0	5		0	
6	1	6	0	6		1	
7	1	7	1	7		1	
DL-1		DL-2		DL-3		SL	

↔
TRANSFER
FROM SL
TO DL-1
OPERATE
DATA OF SL
AND DL-2
TO SL

READ AT
DETERMINATION 2



FIG. 111

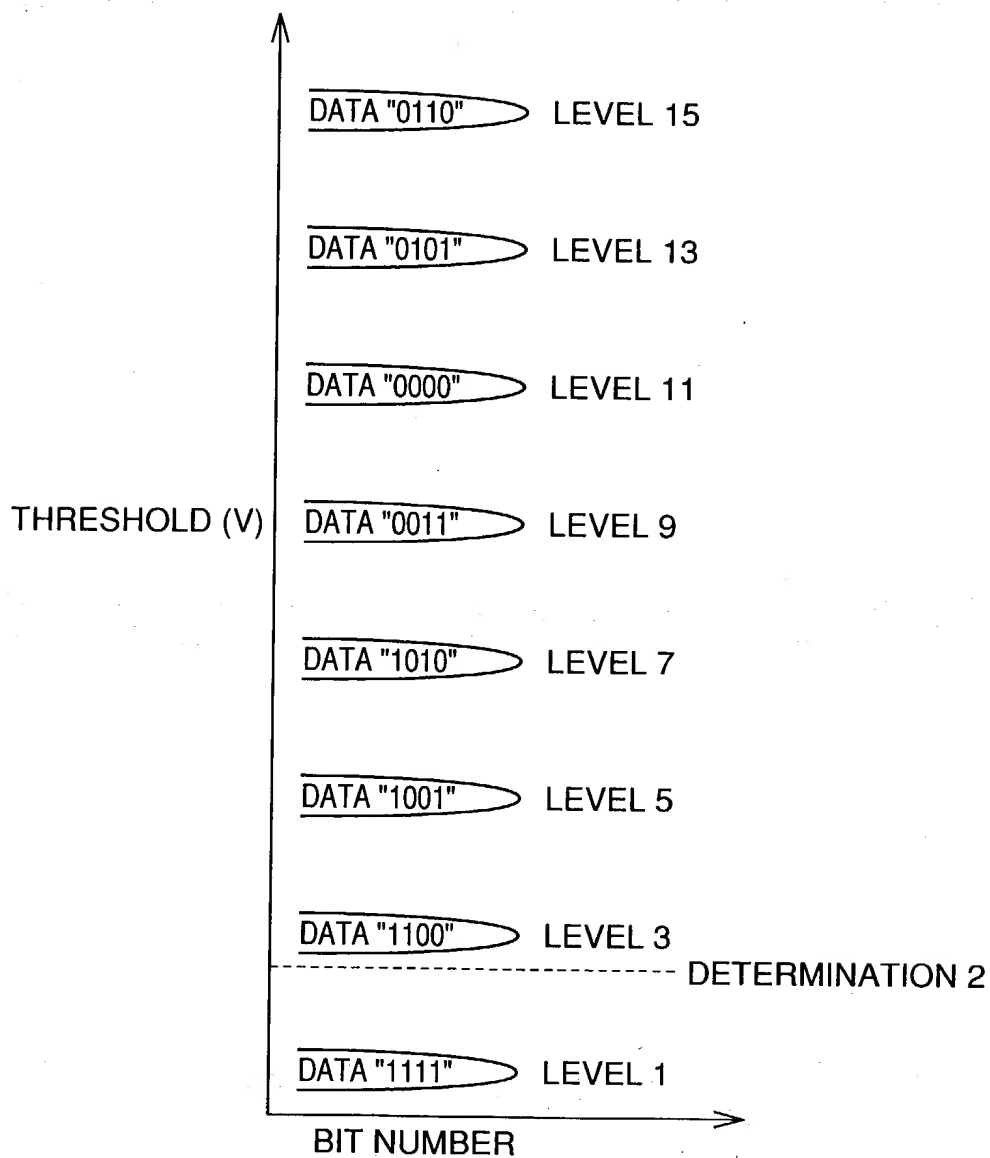




FIG.112

I/O DATA		I/O DATA		I/O DATA	
0	0	0	1	0	
1	0	1	0	1	
2	0	2	0	2	
3	0	3	1	3	
4	0	4	1	4	
5	0	5	0	5	
6	0	6	0	6	
7	0	7	1	7	
0	0	0	1	0	
1	0	1	0	1	
2	0	2	0	2	
3	0	3	1	3	
4	0	4	1	4	
5	0	5	0	5	
6	1	6	0	6	
7	1	7	1	7	
DL-1		DL-2		DL-3	

DATA	
	1
	1
	1
	1
	1
	1
	1
	1
	1
	1
	1
	1
	1
	1
	0
	1
SL	
WRITE LEVEL 2	



FIG.113

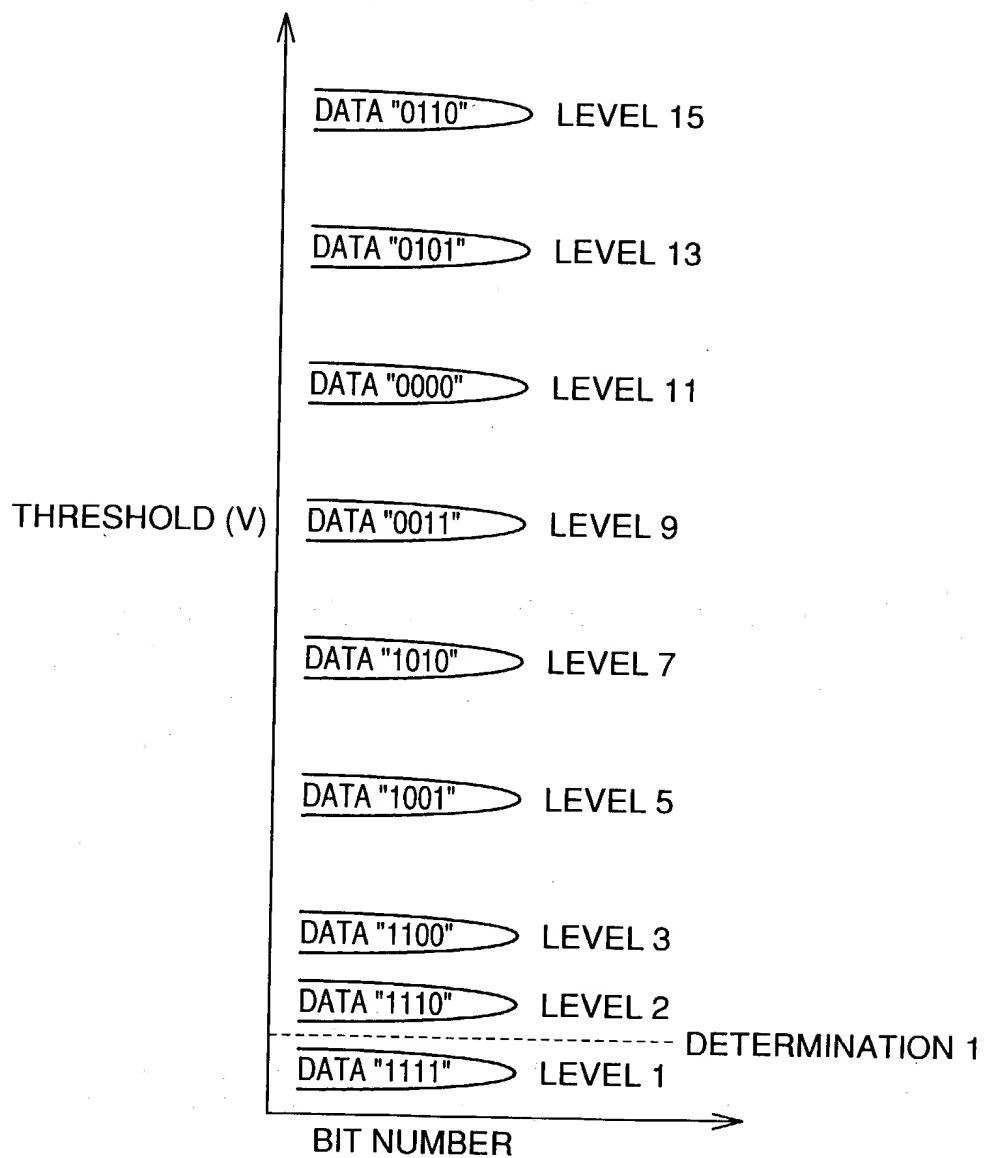




FIG.114

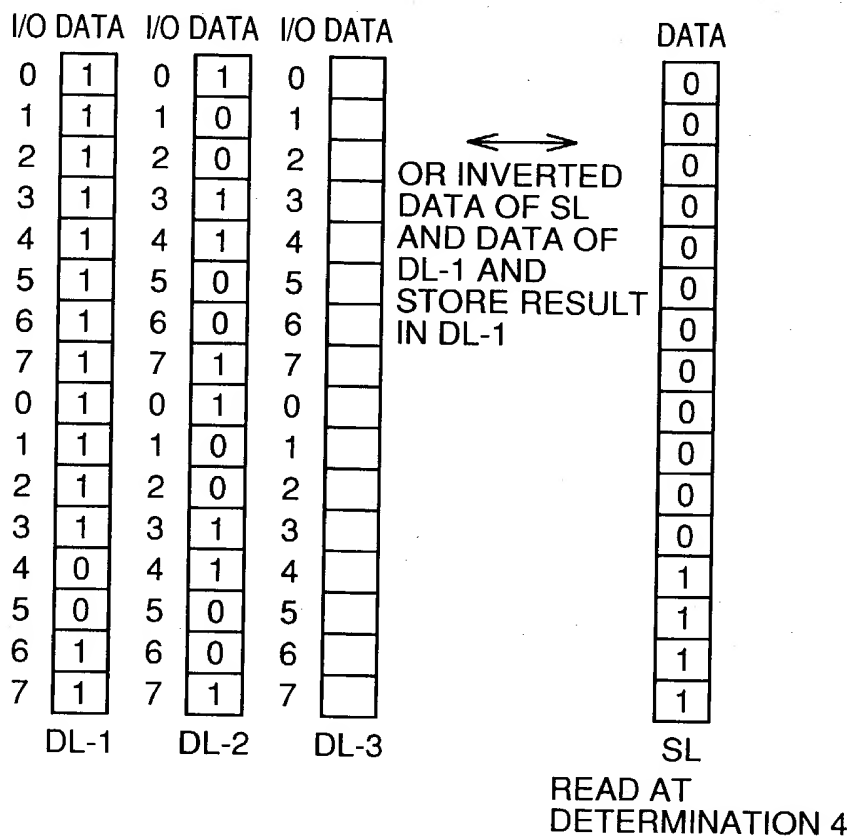


FIG. 115

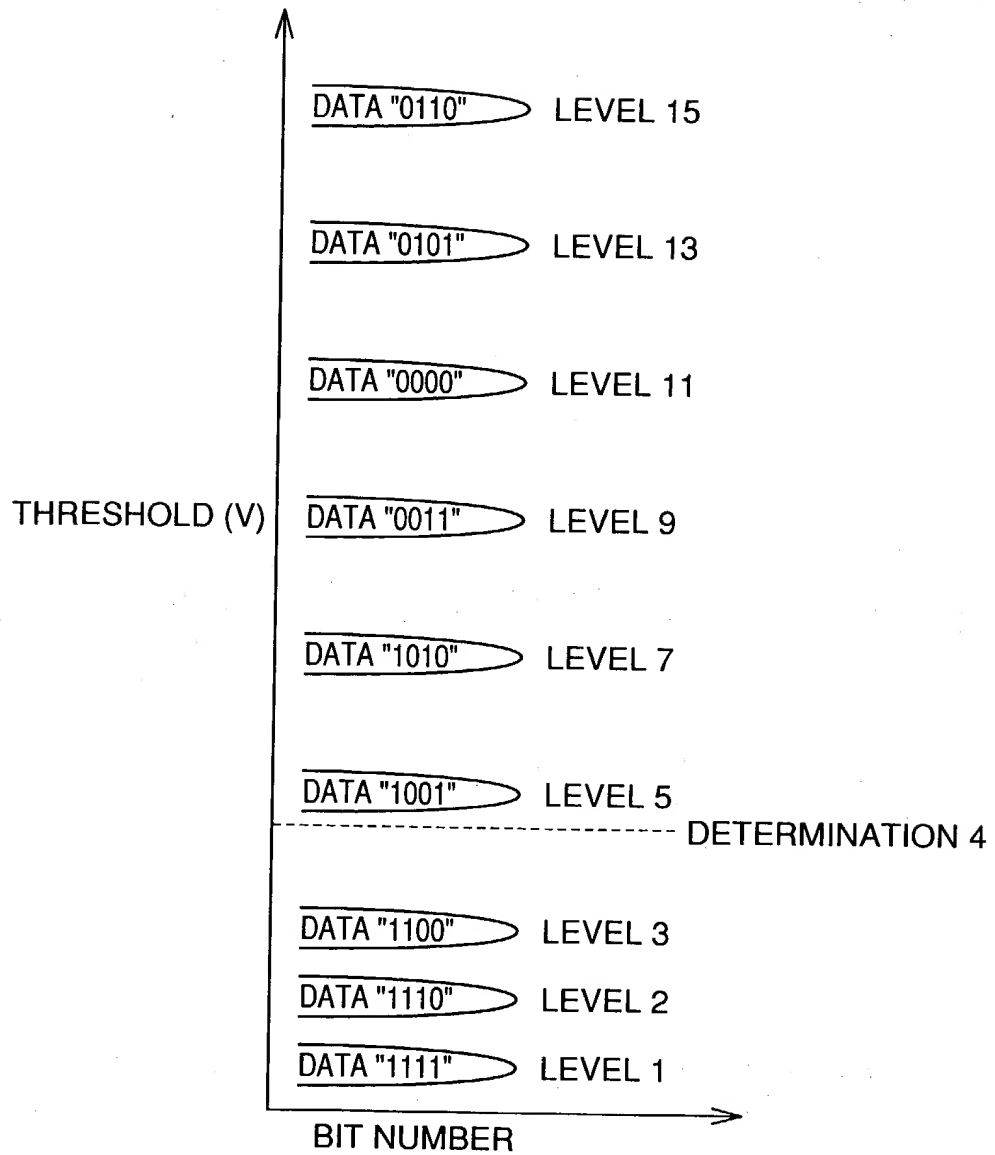




FIG. 116

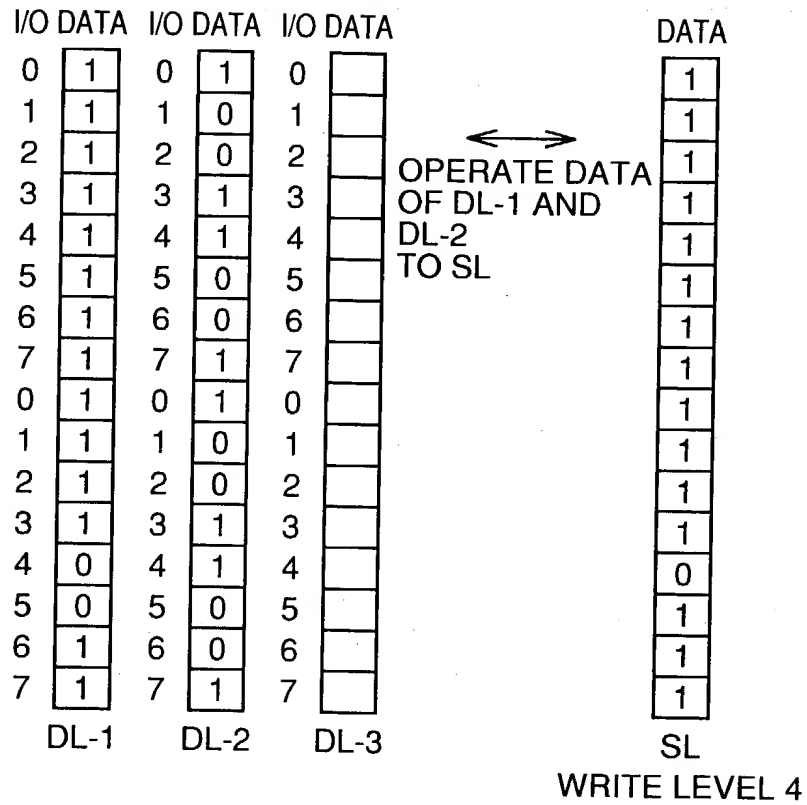




FIG.117

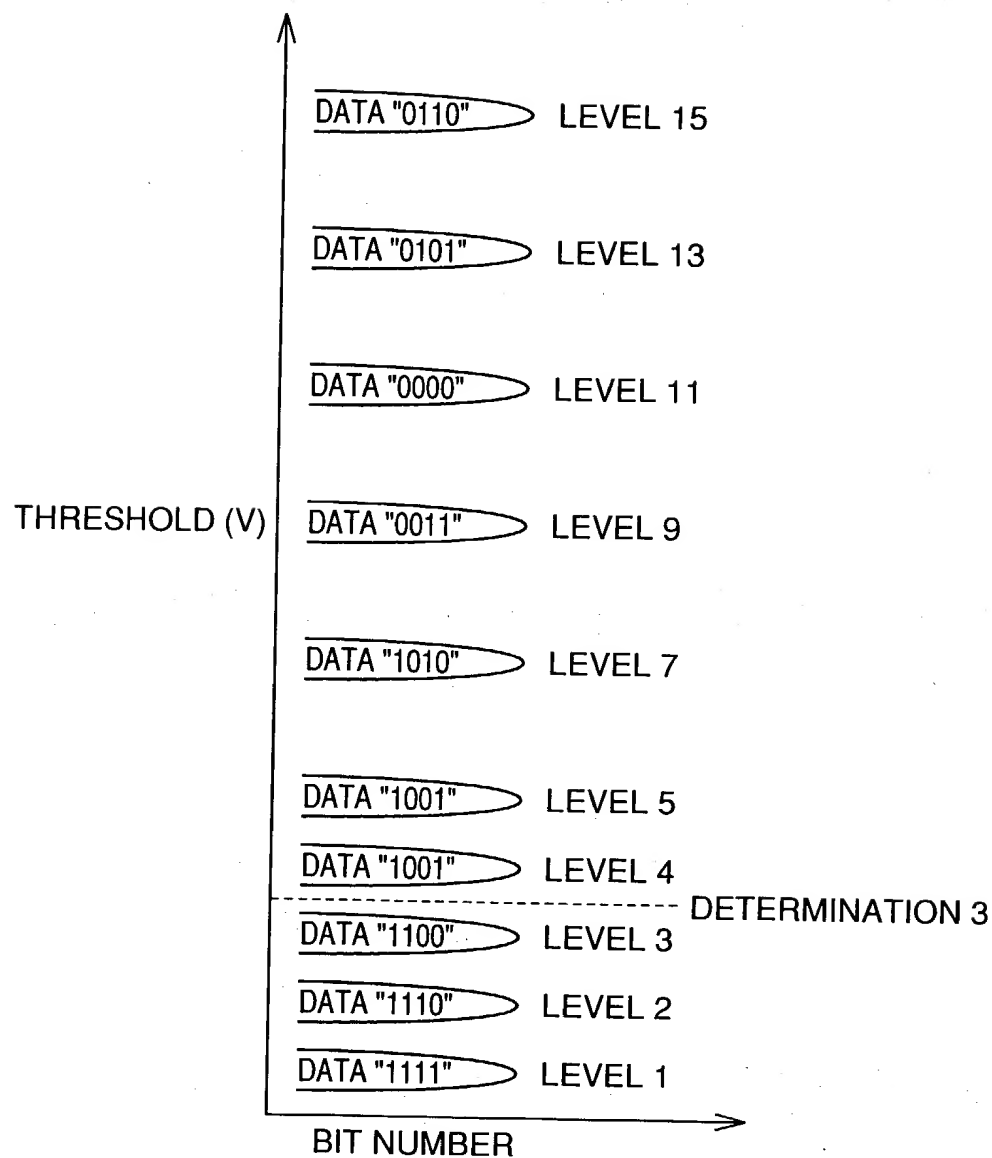


FIG. 118

PRIOR ART

8000

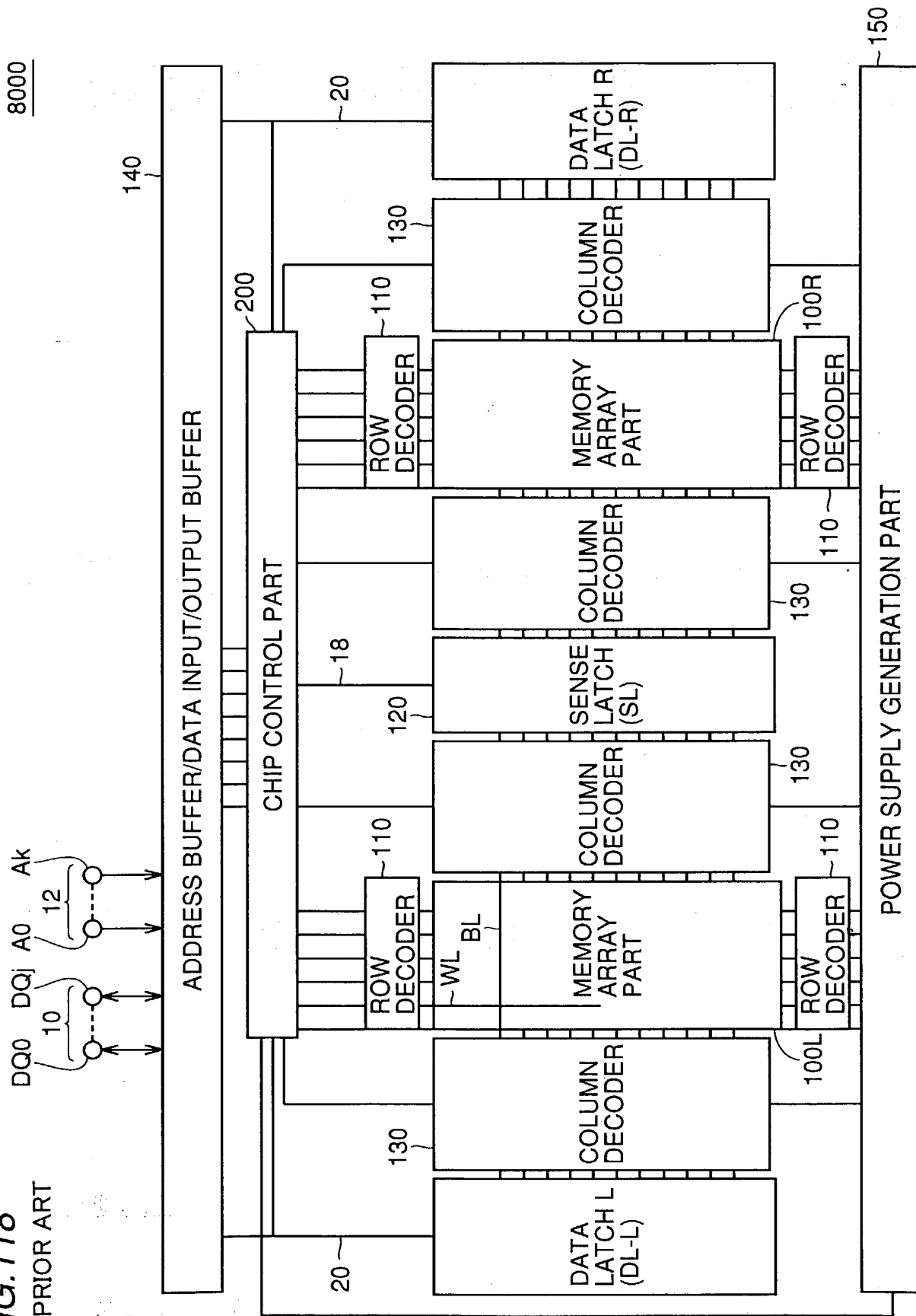




FIG.119 PRIOR ART

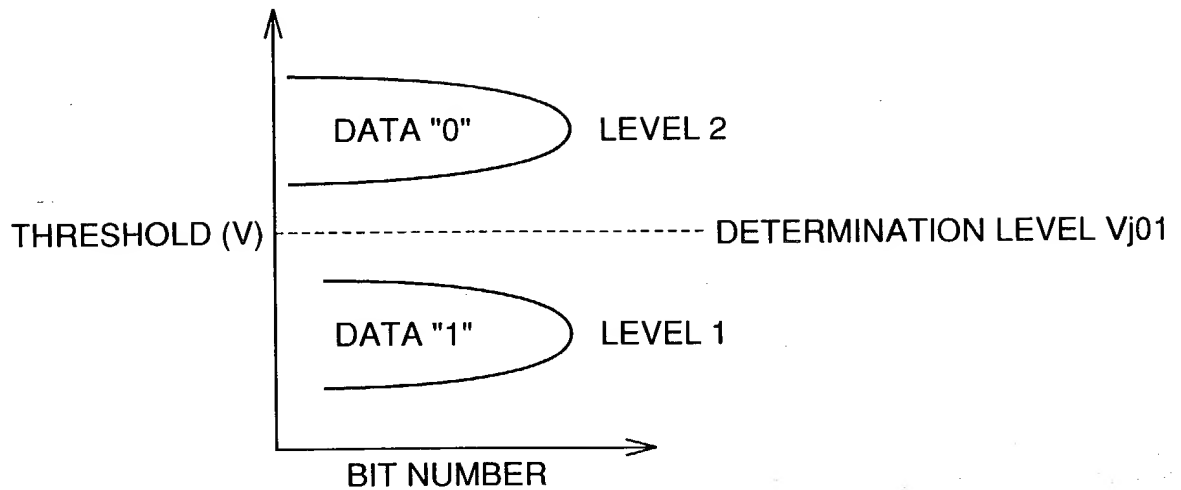


FIG.120 PRIOR ART

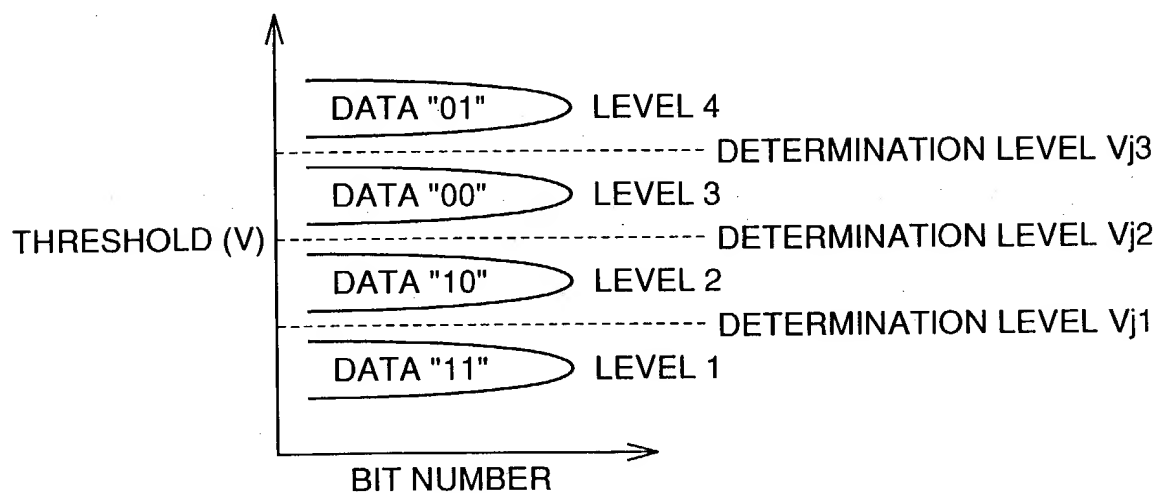




FIG.121 PRIOR ART

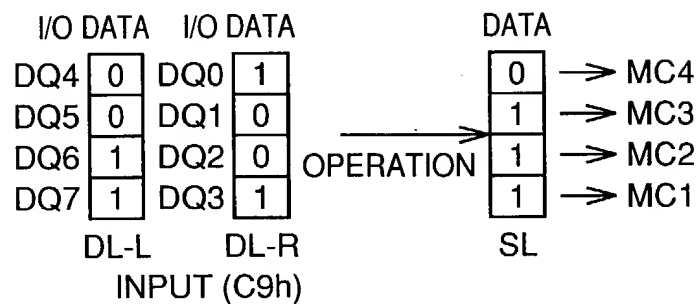


FIG.122 PRIOR ART

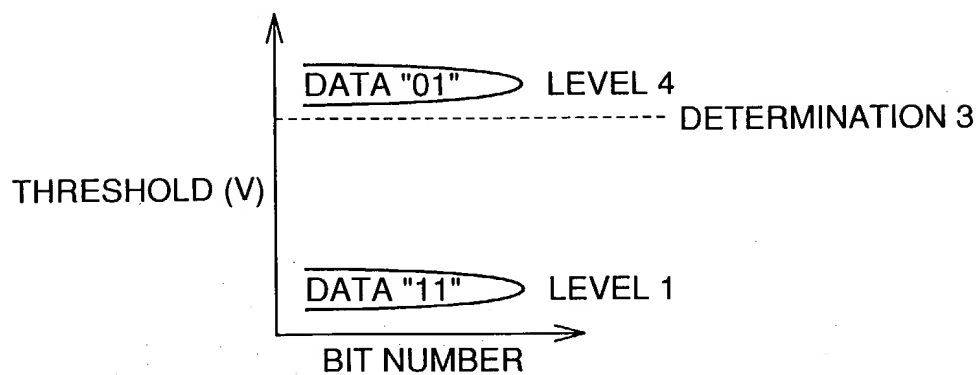




FIG.123 PRIOR ART

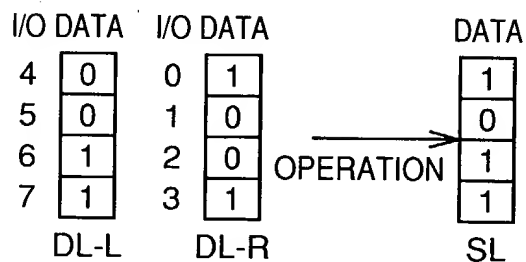


FIG.124 PRIOR ART

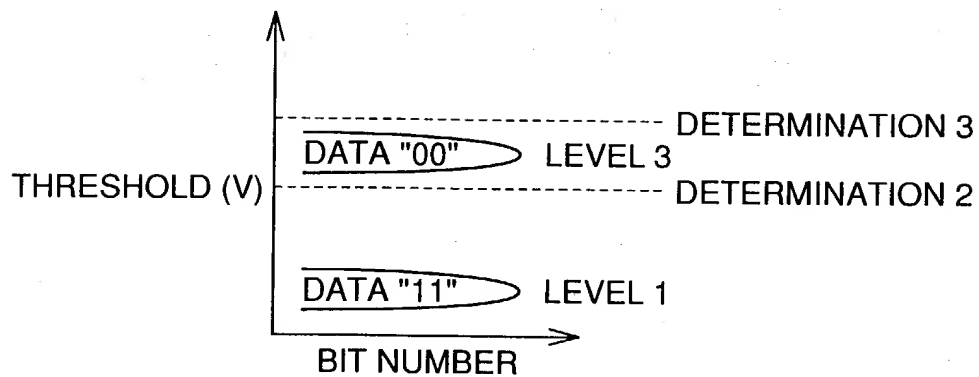




FIG.125 PRIOR ART

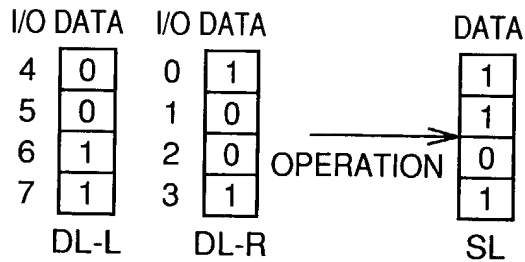


FIG.126 PRIOR ART

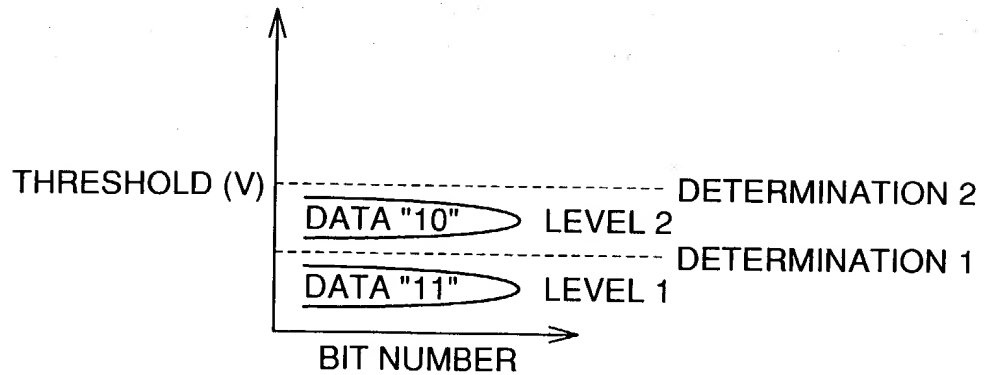


FIG. 127 PRIOR ART

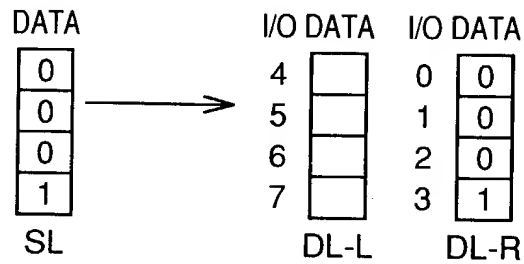


FIG. 128 PRIOR ART

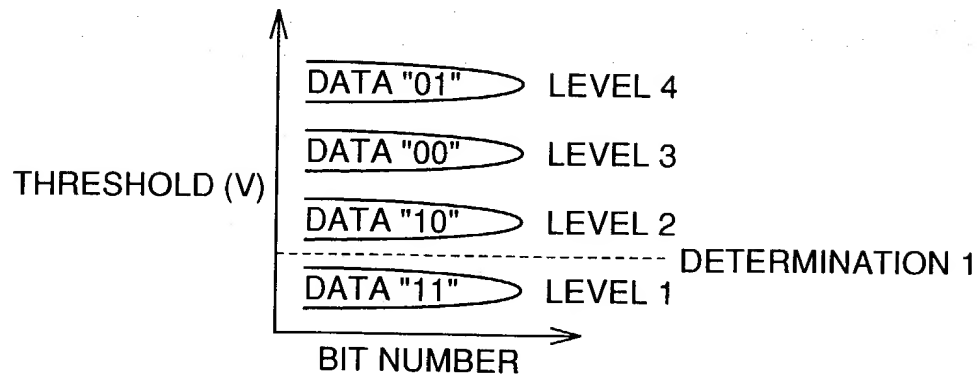


FIG. 129 PRIOR ART

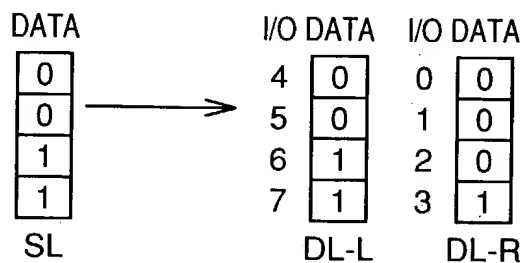


FIG. 130 PRIOR ART

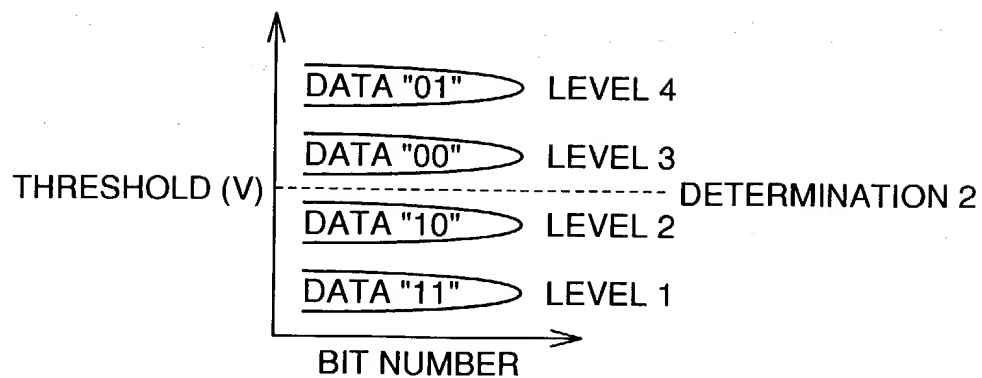




FIG.131 PRIOR ART

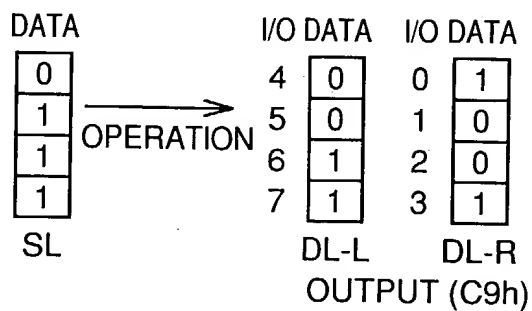


FIG.132 PRIOR ART

